winbond

8-BIT MICROCONTROLLER

Table of Contents-

1. GENERAL DESCRIPTION

The W79E201 is a fast, 8051/52-compatible microcontroller with a redesigned processor core that eliminates wasted clock and memory cycles. Typically, the W79E201 executes instructions 1.5 to 3 times faster than that of the traditional 8051/52, depending on the type of instruction, and the overall performance is about 2.5 times better at the same crystal speed. As a result, with the fully-static CMOS design, the W79E201 can accomplish the same throughput with a lower clock speed, reducing power consumption.

The W79E201 provides one eight-bit digital/analog input port (Port 1) that includes a ten-bit ADC; three eight-bit, bi-directional and bit-addressable I/O ports; a one-bit port P4.0 for external ISP reboot; three 16-bit timers / counters; and one serial port. These peripherals are supported by an eight-source, two-level interrupt capability.

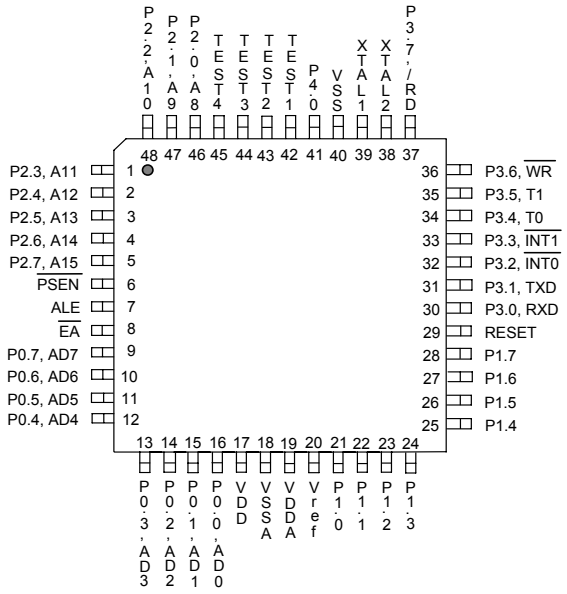
To facilitate programming and verification, the W79E201 contains In-System Programmable (ISP) 16-KB AP Flash EPROM; 4-KB LD Flash EPROM for the loader program in ISP mode; and 256 bytes of RAM. The Flash EPROM allows the program memory to be read and programmed electronically. Once the code is confirmed, it can be protected for security.

2. FEATURES

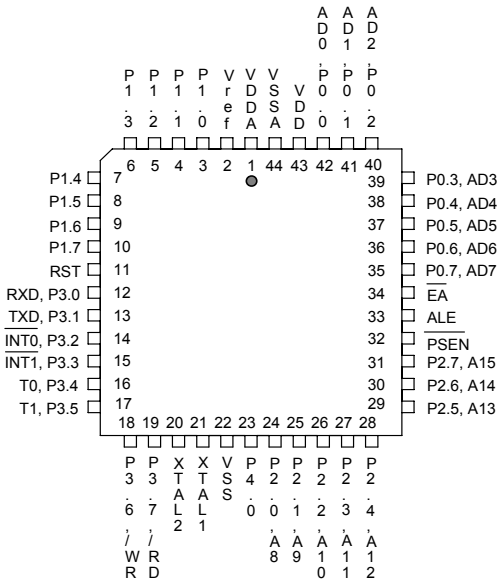
- Fully-static-design 8-bit Turbo 51 CMOS microcontroller up to 16MHz
- 16KB of in-system-programmable Flash EPROM (AP Flash EPROM)
- 4 KB of Auxiliary Flash EPROM for the loader program (LD Flash EPROM)
- 256 bytes of on-chip RAM
- Instruction-set compatible with MSC-51
- Three 8-bit bi-directional ports
- Three 16-bit timers / counters
- 8 interrupt sources with two levels of priority
- One enhanced full-duplex serial port with framing-error detection and automatic address recognition
- Port 0 internal pull-up resistor optional
- Programmable Watchdog Timer
- 6-channel PWM
- Software-programmable access cycle to external RAM/peripherals
- 10-bit ADC with eight-channel analog input or digital input port
- Development Tools:
  - JTAG ICE(In Circuit Emulation) tool
- Packages:
  - Lead Free (RoHS) PLCC 44: W79E201A16PL
  - Lead Free (RoHS) QFP 44: W79E201A16FL
  - Lead Free (RoHS) LQFP 48: W79E201A16LL

3. PIN CONFIGURATION

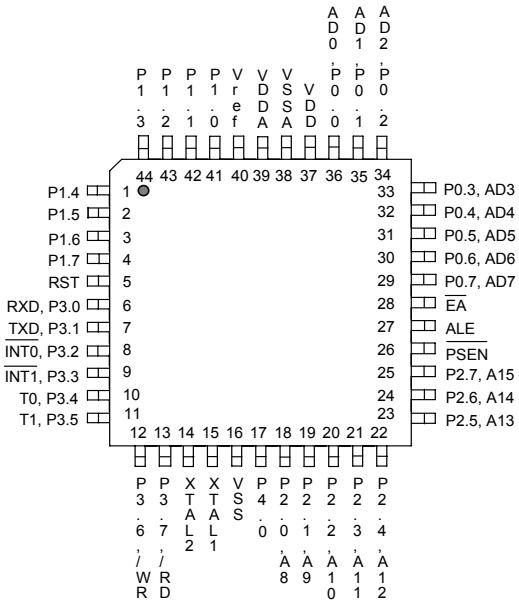
48-Pin LQFP



44-Pin PLCC



44-Pin QFP



4. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
$\overline{EA}$	I H	**EXTERNAL ACCESS ENABLE:** This pin forces the processor to execute from external ROM. It should be kept high to access internal ROM. Note: The ROM address and data are present on the bus, unless the $\overline{EA}$ pin is high and the program counter is within the 16-KB area for internal ROM.
$\overline{PSEN}$	O H	**PROGRAM STORE ENABLE:** $\overline{PSEN}$ enables external ROM devices when data is on the Port-0 address / data bus during fetch and MOVC operations. When internal ROM is accessed, $\overline{PSEN}$ is driven high.
ALE	O H	**ADDRESS LATCH ENABLE:** ALE enables the address latch that separates the address from the data on Port 0.
RST	I L	**RESET:** Set this pin high for two machine cycles while the oscillator is running to reset the device.
XTAL1	I	**CRYSTAL1:** Crystal oscillator input. It may be driven by an external clock.
XTAL2	O	**CRYSTAL2:** Crystal oscillator output. It is the inversion of XTAL1.
V_{SS}	P	**Digital GROUND:** Ground potential
V_{DD}	P	**Digital POWER SUPPLY:** Supply voltage for digital operations.
AV_{DD}	P	**Analog POWER SUPPLY:** Supply voltage for analog operations.
AV_{SS}	P	**Analog GROUND.**
Vref	P	**Vref:** Maximum ADC voltage of analog reference input.
P0.0–P0.7	I/O D(H)	**PORT 0:** Port 0 is an open-drain, bi-directional I/O port. There is an internal pull-up resistor option that is enabled by bit 0 of P0R (8Fh). This port also provides a multiplexed, low-order address / data bus during accesses to external memory.
P1.0–P1.7	I	**PORT 1:** Port 1 is an input port only. This port is also used for 8 channels of analog inputs from ADC0 to ADC7. Furthermore, P1.1 and P1.0 serves T2 and T2EX functions.
P2.0–P2.7	I/O	**PORT 2:** Port 2 is a bi-directional I/O port with weak internal pull-up resistors. This port also provides the upper address bits during accesses to external memory.
P3.0–P3.7	I/O	**PORT 3:** Port 3 is a bi-directional I/O port with weak internal pull-up resistors. Its function is the same as that in the standard 8051/52.
P4.0	I/O	**PORT 4:** A bi-directional I/O port with weak internal pull-up resistors.
TEST1~4	I L	**TEST1~4:** The TEST pins

* **TYPE:** P: power, I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open-drain**.**

5. FUNCTIONAL DESCRIPTION

The W79E201 is instruction-set-compatible, though not pin-compatible, with the 8051/52. It includes most of the standard features of the 8051/52, such as three eight-bit I/O ports, one eight-bit digital or analog input port, three 16-bit timers / counters, one full-duplex serial port and interrupt sources, and it has a few extra peripherals and features as well.

The W79E201 features a redesigned, eight-bit core processor that eliminates wasted clock and memory cycles. It improves the speed and performance not just by running at high frequency but also by reducing the machine-cycle duration from the standard-8051/52 period of twelve clock cycles to four clock cycles for the majority of instructions. This improves the performance by an average of 1.5 to 3 times. The W79E201 can also adjust the duration of the MOVX instruction, anywhere from two machine cycles to nine machine cycles, to work efficiently with fast and slow external RAM and peripheral devices.

5.1 I/O Ports

The W79E201 has one eight-bit digital or analog input port, three eight-bit I/O ports and one extra, one-bit port at P4.0.

Port 0 can also be used as an address / data bus when a program is running in external memory or when external memory or devices are accessed by MOVC or MOVX instructions. In these cases, it has strong pull-up and pull-down resistors and does not need any external resistors. Otherwise, it can be used as a general I/O port with open-drain circuits.

Port 1 is the only input port that can be connected to the ADC. Port 2 is used chiefly as the upper eight bits of the address bus when port 0 is used as an address / data bus, and, as an address bus, it also has strong pull-up and pull-down resistors. Port 3 acts as an I/O port with additional, alternative functions, and Port 4.0 is a general-purpose I/O port similar to Port 3.

5.2 Serial I/O

The W79E201 has one enhanced serial port that is functionally similar to the original 8051/52 serial port. However, the W79E201 serial port can operate in different modes to obtain timing similarity as well. It also has two enhancements, Automatic Address Recognition and Frame Error Detection.

5.3 Timers

The W79E201 has three 16-bit timers that are functionally similar to the timers of the 8051/52 family. When used as timers, they can run at either four clocks or twelve clocks per count, thus providing the user with the option of emulating the timing of the original 8051/52. The W79E201 also has a Watchdog Timer that acts as a system monitor or a long-period timer.

5.4 Interrupts

The Interrupt structure in the W79E201 is slightly different from that of the standard 8051/52. Because of additional features and peripherals, the number of interrupt sources and vectors is higher. The W79E201 provides eight interrupt resources–two external interrupt sources, three timer interrupts, one serial I/O interrupt, one ADC interrupt and one watchdog timer interrupt—with two priority levels.

5.5 Power Management

Like the standard 8051/52, the W79E201 has IDLE and POWER DOWN modes of operation. In POWER DOWN mode, all of the peripheral clocks are stopped, and chip operation stops completely. This mode consumes the least amount of power.

5.6 Memory Organization

The W79E201 separates memory into two sections, Program Memory and Data Memory. Program Memory stores instruction op-codes, while Data Memory stores data or memory-mapped devices.

Program Memory

On the standard 8051/52, only 64 KB of Program Memory can be addressed, and, in the W79E201, this area is the 16-KB Flash EPROM (AP Flash EPROM). All instructions are fetched from this area, and the MOVC instruction can also access this region. There is an auxiliary 4-KB Flash EPROM (LD Flash EPROM), where the loader program for In-System Programming (ISP) resides. The AP Flash EPROM is re-programmed by serial or parallel download according to this loader program.

Data Memory

The W79E201 can access up to 64 KB of external Data Memory. This memory is accessed by MOVX instructions, and any MOVX instructions to 0000H through FFFFH go to the expanded bus on Ports 0 and 2. This is the default condition.

The W79E201 also has the standard 256 bytes of on-chip Scratchpad RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing. Since the Scratchpad RAM is only 256 bytes, it can be used only when data contents are small.

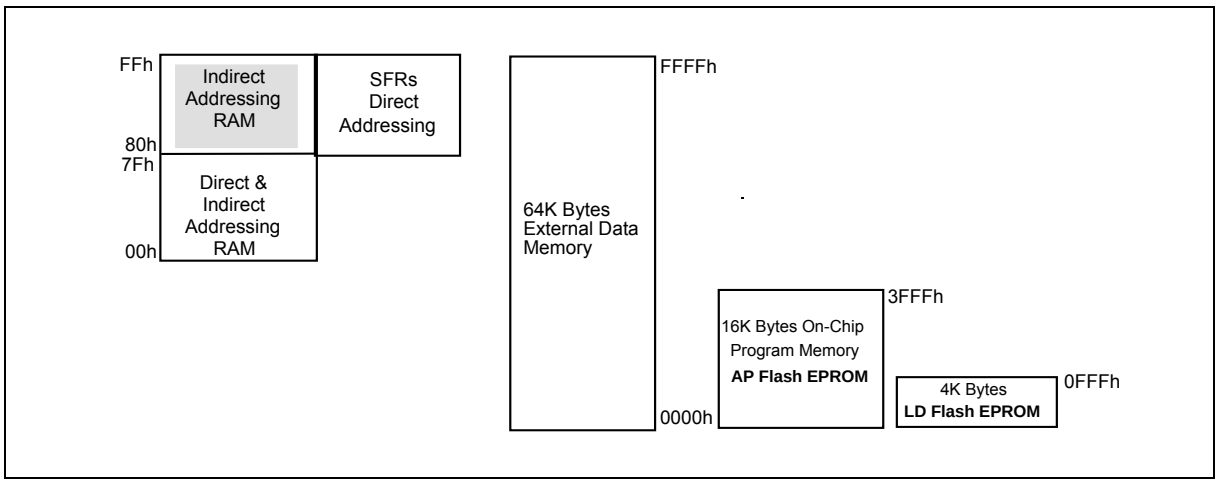


Figure 5-1 Memory Map

6. SPECIAL FUNCTION REGISTERS

The W79E201 uses Special Function Registers (SFR) to control and monitor peripherals. The SFR reside in register locations 80-FFh and are only accessed by direct addressing. The W79E201 contains all the SFR present in the standard 8051/52, as well as some additional SFR, and, in some cases, unused bits in the standard 8051/52 have new functions. SFR whose addresses end in 0 or 8 (hex) are bit-addressable. The following table of SFR is condensed, with eight locations per row. Empty locations indicate that there are no registers at these addresses. When a bit or register is not implemented, it reads high.

Table 1 Special Function Register Location Table

F8	EIP							
F0	B							
E8	EIE							
E0	ACC	ADCCON	ADCH		ADCCEN			
D8	WDCON	PWMP	PWM0	PWM1	PWMCON1	PWM2	PWM3	
D0	PSW							
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	PWMCON2	PWM4
C0				PWM5	PMR	Status		TA
B8	IP	SADEN						
B0	P3							
A8	IE	SADDR			SFRAL	SFRAH	SFRFD	SFRCN
A0	P2					P4		
98	SCON	SBUF						CHPCON
90	P1							
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	P0R
80	P0	SP	DPL	DPH				PCON

Note: The SFRs in the column with dark borders are bit-addressable.

Port 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

Port 0 is an open-drain, bi-directional I/O port after chip is reset. Besides, it has internal pull-up resisters enabled by setting P0UP of P0R (8FH) to high. This port also provides a multiplexed, low-order address/data bus when the W79E201 accesses external memory.

Stack Pointer

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

The Stack Pointer stores the address in Scratchpad RAM where the stack begins. It always points to the top of the stack.

Data Pointer Low

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

This is the low byte of the standard-8051/52, 16-bit data pointer.

Data Pointer High

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

This is the high byte of the standard-8051/52, 16-bit data pointer.

Power Control

Bit:	7	6	5	4	3	2	1	0
	SM0D	SMOD0	-	-	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial-port baud rate in modes 1, 2 and 3.
6	SMOD0	0: Disable Framing Error Detection. SCON.7 acts as per the standard 8051/52 function. 1: Enable Framing Error Detection. SCON.7 indicates a Frame Error and acts as the FE flag.
5-4	-	Reserved
3	GF1	General-purpose user flag.
2	GF0	General-purpose user flag.
1	PD	1: Go into POWER DOWN mode. In this mode, all clocks and program execution are stopped.
0	IDL	1: Go into IDLE mode. In this mode, the CPU clock stops, so program execution stops too. However, the clock to the serial port, ADC, timer and interrupt blocks does not stop, so these blocks continue operating.

Timer Control

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program executes the Timer-1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 run control: This bit turns the Timer 1 on or off.
5	TF0	Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program executes the Timer-0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 run control: This bit turns Timer 0 on or off.
3	IE1	Interrupt 1 Edge Detect: Set by hardware when an edge / level is detected on $\overline{INT1}$. This bit is cleared by the hardware when the ISR is executed only if the interrupt is edge-triggered. Otherwise, it follows the pin.
2	IT1	Interrupt 1 type control: Specify falling-edge or low-level trigger for $\overline{INT1}$.
1	IE0	Interrupt 0 Edge Detect: Set by hardware when an edge / level is detected on $\overline{INT0}$. This bit is cleared by the hardware when the ISR is executed only if the interrupt is edge-triggered. Otherwise, it follows the pin.
0	IT0	Interrupt 0 type control: Specify falling-edge or low-level trigger for $\overline{INT0}$.

Timer Mode Control

Bit:	7	6	5	4	3	2	1	0
	GATE	$C/\overline{T}$	M1	M0	GATE	$C/\overline{T}$	M1	M0

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When clear, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 is set.
6	$C/\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the Tx pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.

Continued

BIT	NAME	FUNCTION
3	GATE	Gating control: When this bit is set, Timer 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When clear, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the Tx pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	Mode
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer-0 control bits. TH0 is an 8-bit timer only controlled by Timer-1 control bits. (Timer 1) Timer/Counter 1 is stopped.

Timer 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

TL0.7–0: Timer 0 LSB

Timer 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

TL1.7–0: Timer 1 LSB

Timer 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

TH0.7–0: Timer 0 MSB

Timer 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

TH1.7–0: Timer 1 MSB

Clock Control

Bit:	7	6	5	4	3	2	1	0
	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7	WD1	Watchdog Timer mode select bit 1. See table below.
6	WD0	Watchdog Timer mode select bit 0. See table below.
5	T2M	Timer 2 clock select: 1: divide-by-4 clock 0: divide-by-12 clock
4	T1M	Timer 1 clock select: 1: divide-by-4 clock 0: divide-by-12 clock
3	T0M	Timer 0 clock select: 1: divide-by-4 clock 0: divide-by-12 clock
2	MD2	Stretch MOVX select bit 2: MD2, MD1, and MD0 select the stretch value for the MOVX instruction. The $\overline{RD}$ or $\overline{WR}$ strobe is stretched by the selected interval, which enables the W79E201 to access faster or slower external memory devices or peripherals without the need for external circuits. By default, the stretch value is one. See table below. (Note: When accessing on-chip SRAM, these bits have no effect, and the MOVX instruction always takes two machine cycles.)
1	MD1	Stretch MOVX select bit 1. See MD2.
0	MD0	Stretch MOVX select bit 0. See MD2.

WD1, WD0: Mode Select bits:

These bits determine the time-out periods for the Watchdog Timer. The reset time-out period is 512 clocks more than the interrupt time-out period.

WD1	WD0	INTERRUPT TIME-OUT	RESET TIME-OUT
0	0	2^{17}	2^{17} + 512
0	1	2^{20}	2^{20} + 512
1	0	2^{23}	2^{23} + 512
1	1	2^{26}	2^{26} + 512

MD2, MD1, MD0: Stretch MOVX select bits:

MD2	MD1	MD0	STRETCH VALUE	MOVX DURATION
0	0	0	0	2 machine cycles
0	0	1	1	3 machine cycles *(Default)*
0	1	0	2	4 machine cycles
0	1	1	3	5 machine cycles
1	0	0	4	6 machine cycles
1	0	1	5	7 machine cycles
1	1	0	6	8 machine cycles
1	1	1	7	9 machine cycles

Port 0 pull-up resister

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	P0UP

Mnemonic: P0R Address: 8Fh

BIT	NAME	FUNCTION
7~1	-	Reserved
0	P0UP	Port 0 Pull-Up Resistor 0: No pull-up resistor 1: Pull-up resistor (~10 KΩ)

Port 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7–0: General-purpose digital input port or analog input port AD0~AD7. For digital input, port-read instructions read the port pins, while read-modify-write instructions read the port latch. Additional functions are described below. This port is also used for 8 channels of analog inputs from ADC0 to ADC7.

BIT	NAME	FUNCTION
1	P1.1	T2 : External Input for Timer/Counter 2
0	P1.0	T2EX : Timer/Counter 2 Capture/Reload Trigger

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial Port mode select bit 0 or Framing Error Flag: This bit is controlled by the SMOD0 bit in the PCON register. (SM0) See table below. (FE) This bit indicates an invalid stop bit. It must be manually cleared by software.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Serial Port Clock or Multi-Processor Communication. (Mode 0) This bit controls the serial port clock. If set to zero, the serial port runs at a divide-by-12 clock of the oscillator. This is compatible with the standard 8051/52. (Mode 1) If SM2 is set to one, RI is not activated if a valid stop bit is not received. (Modes 2 / 3) This bit enables multi-processor communication. If SM2 is set to one, RI is not activated if RB8, the ninth data bit, is zero.
4	REN	Receive enable: 1: Enable serial reception 0: Disable serial reception
3	TB8	(Modes 2 / 3) This is the 9th bit to transmit.
2	RB8	(Mode 0) No function. (Mode 1) If SM2 = 0, RB8 is the stop bit that was received. (Modes 2 / 3) This is the 9th bit that was received.
1	TI	Transmit interrupt flag: This flag is set by the hardware at the end of the 8th bit in mode 0 or at the beginning of the stop bit in the other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by the hardware at the end of the 8th bit in mode 0 or halfway through the stop bits in the other modes during serial reception. However, SM2 can restrict this behavior. This bit can only be cleared by software.

SM0, SM1: Mode Select bits:

SM0	SM1	MODE	DESCRIPTION	LENGTH	BAUD RATE
0	0	0	Synchronous	8	Tclk divided by 4 or 12
0	1	1	Asynchronous	10	Variable
1	0	2	Asynchronous	11	Tclk divided by 32 or 64
1	1	3	Asynchronous	11	Variable

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

SBUF.7–0: Serial data in the serial port is read from or written to this location. It actually consists of two separate 8-bit registers, the receive register and the transmit buffer. Read accesses get data from the receive register, and write accesses write to the transmit buffer.

ISP Control Register

Bit:	7	6	5	4	3	2	1	0
	SWRST/ REBOOT	-	LDAP	-	-	-	FBOOTSL	FPROGEN

Mnemonic: CHPCON Address: 9Fh

BIT	NAME	FUNCTION
7	SWRST/ REBOOT	Set this bit to reset the device. This has the same effect as asserting the RST pin. The microcontroller returns to its initial state, and this bit is cleared automatically. Reading this bit indicates whether or not the device is in ISP hardware reboot mode.
6	-	Reserved
5	LDAP	This bit is read-only. 1: Device is running the program in LD Flash EPROM 0: Device is running the program in AP Flash EPROM
4-2	-	Reserved
1	FBOOTSL	Program Location Selection. This bit should be set before entering ISP mode. 1: Run the program in LD Flash EPROM. 0: Run the program in AP Flash EPROM.
0	FPROGEN	FLASH EPROM Programming Enable. 1: Enable in-system programming mode. The erase, program and read operations are executed according to various SFR settings. In this mode, the device runs in IDLE state, so PCON.1 has no effect. 0: Disable in-system programming mode. The device returns to normal operations, and PCON.1 is functional again.

Port 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

P2.7-0: Port 2 is a bi-directional I/O port with internal pull-up resistors. This port also provides the upper address bits for accesses to external memory.

Port 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	P4.0

Mnemonic: P4 Address: A5h

P4.0:

When security bit B3 is 0, P4.0 is the reboot pin.

When security bit B3 is 1, P4.0 is an I/O pin.

Interrupt Enable

Bit:	7	6	5	4	3	2	1	0
	EA	EADC	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/disable all interrupts.
6	EADC	Enable ADC interrupt.
5	ET2	Enable Timer 2 interrupt.
4	ES	Enable Serial Port interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

Slave Address

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR Address: A9h

The SADDR should be programmed to the given or broadcast address for the serial ports to which a slave processor is designated.

ISP Address Low Byte

Bit:	7	6	5	4	3	2	1	0
	SFRAL.7	SFRAL.6	SFRAL.5	SFRAL.4	SFRAL.3	SFRAL.2	SFRAL.1	SFRAL.0

Mnemonic: SFRAL Address: ACh

Low-byte destination address for In-System Programming operations. SFRAH and SFRAL are specific ROM locations for erase, program or read operations.

ISP Address High Byte

Bit:	7	6	5	4	3	2	1	0
	SFRAH.7	SFRAH.6	SFRAH.5	SFRAH.4	SFRAH.3	SFRAH.2	SFRAH.1	SFRAH.0

Mnemonic: SFRAH Address: ADh

High-byte destination address for In-System Programming operations. SFRAH and SFRAL are specific ROM locations for erase, program or read operations.

ISP Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SFRFD.7	SFRFD.6	SFRFD.5	SFRFD.4	SFRFD.3	SFRFD.2	SFRFD.1	SFRFD.0

Mnemonic: SFRFD Address: AEh

In ISP mode, bytes read from ROM and bytes written to ROM go through SFRFD

ISP Operation Modes

Bit:	7	6	5	4	3	2	1	0
	-	WFWIN	OEN	CEN	CTRL3	CTRL2	CTRL1	CTRL0

Mnemonic: SFRCN Address: AFh

BIT	NAME	FUNCTION
7	-	Reserved
6	WFWIN	On-chip Flash EPROM bank select for in-system programming. This bit should be set by the loader program in ISP mode. 0: 16-KB Flash EPROM is the destination for re-programming. 1: 4-KB Flash EPROM is the destination for re-programming.
5	OEN	Flash EPROM output is enabled.
4	CEN	Flash EPROM chip is enabled.
3~0	CTRL[3:0]	The flash control signals. See table below.

WFWIN, OEN, CEN, CTRL[3:0]: ISP Instruction select bits:

ISP MODE	WFWIN	OEN	CEN	CTRL<3:0>	SFRAH, SFRAL	SFRFD
Erase 4-KB LD FLASH PROM	1	1	0	0010	X	X
Erase 16-K AP FLASH EPROM	0	1	0	0010	X	X
Program 4-KB LD FLASH EPROM	1	1	0	0001	Address in	Data in
Program 16-KB AP FLASH EPROM	0	1	0	0001	Address in	Data in
Read 4-KB LD FLASH EPROM	1	0	0	0000	Address in	Data out
Read 16-KB AP FLASH EPROM	0	0	0	0000	Address in	Data out

Port 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: General-purpose I/O port. Each pin also has an alternative input or output function, which is described below.

BIT	NAME	FUNCTION
7	P3.7	$\overline{RD}$ strobe for reading from external RAM
6	P3.6	$\overline{WR}$ strobe for writing to external RAM
5	P3.5	Timer 1 external count input
4	P3.4	Timer 0 external count input
3	P3.3	External interrupt 1 $\overline{INT1}$
2	P3.2	External interrupt 0 $\overline{INT0}$
1	P3.1	TxD: Serial port 0 output
0	P3.0	RxD: Serial port 0 input

Interrupt Priority

Bit:	7	6	5	4	3	2	1	0
	-	PADC	PT2	PS	PT1	PX1	PT0	PX0

Mnemonic: IP Address: B8h

BIT	NAME	FUNCTION
7	-	Reserved. This bit reads high.
6	PADC	1: Set the priority of the ADC interrupt to the highest level.
5	PT2	1: Set the priority of the Timer 2 interrupt to the highest level.
4	PS	1: Set the priority of the Serial Port interrupt to the highest level.
3	PT1	1: Set the priority of the Timer 1 interrupt to the highest level.
2	PX1	1: Set the priority of external interrupt 1 to the highest level.
1	PT0	1: Set the priority of the Timer 0 interrupt to the highest level.
0	PX0	1: Set the priority of external interrupt 0 to the highest level.

Slave Address Mask Enable

Bit:	7	6	5	4	3	2	1	0
	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0

Mnemonic: SADEN Address: B9h

BIT	NAME	FUNCTION
7~0	SADEN	This register enables the Automatic Address Recognition feature for the serial port. When a bit in SADEN is set to 1, the same bit in SADDR is compared to incoming serial data. When a bit in SADEN is set to 0, the same bit becomes a "don't care" condition in the comparison. Disable Automatic Address Recognition by setting all the bits in SADEN to 0.

PWM 5 Register

Bit:	7	6	5	4	3	2	1	0
	PWM5.7	PWM5.6	PWM5.5	PWM5.4	PWM5.3	PWM5.2	PWM5.1	PWM5.0

Mnemonic: PWM 5 Address: C3h

Power Management Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	ALE-OFF	-	-

Mnemonic: PMR Address: C4h

BIT	NAME	FUNCTION
7~3	-	Reserved.
2	ALE-OFF	0: ALE expression is enabled during on-board program and data accesses. 1: ALE expression is disabled. Keep the logic in the high state. External memory accesses automatically enable ALE, regardless of ALE-OFF.
1~0	-	Reserved.

Status Register

Bit:	7	6	5	4	3	2	1	0
	-	HIP	LIP	-	-	-	SPTA0	SPRA0

Mnemonic: STATUS Address: C5h

BIT	NAME	FUNCTION
7	-	Reserved.
6	HIP	High-Priority Interrupt Status. When set, it indicates that the software is servicing a high-priority interrupt. This bit is cleared when the program executes the corresponding RETI instruction.
5	LIP	Low-Priority Interrupt Status. When set, it indicates that the software is servicing a low-priority interrupt. This bit is cleared when the program executes the corresponding RETI instruction.
4-2	-	Reserved.
1	SPTA0	Serial-Port Transmit Activity. This bit is set when the serial port is transmitting data. It is cleared when the TI bit is set by the hardware.
0	SPRA0	Serial-Port Receive Activity. This bit is set when the serial port is receiving data. It is cleared when the RI bit is set by the hardware.

Timed Access

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA Address: C7h

TA: This register controls the access to protected bits. To access protected bits, the program must write AAH, followed immediately by 55H, to TA. This opens a window for three machine cycles, during which the program can write to protected bits.

Timer 2 Control

Bit:	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$CP/\overline{RL2}$

Mnemonic: T2CON Address: C8h

BIT	NAME	FUNCTION
7	TF2	Timer 2 Overflow flag: This bit is set when Timer 2 overflows. It is also set when the count is equal to the capture register in down-count mode. It can be set by the hardware only if RCLK and TCLK are both 0, and it can be set or cleared by software.
6	EXF2	Timer 2 External flag: A negative transition on the T2EX pin (P1.1) or a timer 2 underflow / overflow sets this flag according to the CP/RL2, EXEN2 and DCEN bits. This bit can also be set by the software. If set by a negative transition, this flag must be cleared by software. If set by a negative transition or by software, a Timer 2 interrupt is generated, if enabled.
5	RCLK	Receive Clock flag: This bit determines the serial-port time base when receiving data in Serial Port modes 1 or 3. 0: The Timer 1 overflow is used for baud-rate generation 1: The Timer 2 overflow is used for baud-rate generation, forcing Timer 2 into baud-rate generator mode.
4	TCLK	Transmit Clock flag: This bit determines the serial-port time base when transmitting data in Serial Port modes 1 or 3. 0: The Timer 1 overflow is used for baud-rate generation 1: The Timer 2 overflow is used for baud-rate generation, forcing Timer 2 into baud-rate generator mode.
3	EXEN2	Timer 2 External Enable: This bit enables the capture / reload function on the T2EX pin, as long as Timer 2 is not generating baud clocks for the serial port. 0: Ignore T2EX. 1: Negative transitions on T2EX result in capture or reload.
2	TR2	Timer 2 Run Control: This bit enables / disables Timer 2. When disabled, Timer 2 preserves the current values in TH2 and TL2.
1	$\overline{C/T2}$	Counter / Timer select: 0: Timer 2 operates as a timer at a speed depending on T2M bit (CKCON.5) 1: Timer 2 counts negative edges on the T2EX pin. Regardless of this bit, Timer 2 may be forced into baud-rate generator mode.
0	$\overline{CP/RL2}$	Capture / Reload select, when Timer 2 overflows or when a falling edge is detected on T2EX (and EXEN2 = 1). 0: Auto-reload Timer 2 1: Capture in Timer 2 If RCLK or TCLK is set, this bit does not function, and Timer 2 runs in auto-reload mode following each overflow.

Timed 2 Mode Control

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	T2CR	-	-	DCEN

Mnemonic: T2MOD Address: C9h

BIT	NAME	FUNCTION
7~4	-	Reserved.
3	T2CR	Timer 2 Capture Reset. In Timer-2 Capture Mode, 1: Automatically reset Timer 2 once the Timer 2 capture registers have captured the values in Timer 2.
2~1	-	Reserved.
0	DCEN	Down Count Enable: This bit controls the direction that Timer 2 counts in 16-bit auto-reload mode.

Timer 2 Capture LSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Mnemonic: RCAP2L Address: CAh

RCAP2L:

(Capture mode) This register captures the LSB of Timer 2 (TL2).

(Auto-reload mode) This register is the LSB of the 16-bit reload value.

Timer 2 Capture MSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H Address: CBh

RCAP2H:

(Capture mode) This register captures the MSB of Timer 2 (TH2).

(Auto-reload mode) This register is the MSB of the 16-bit reload value.

Timer 2 LSB

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2 Address: CCh

TL2: Timer 2 LSB

Timer 2 MSB

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2 Address: CDh

TH2: Timer 2 MSB

PWM 4~5 Control Register 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWM5OE	PWM4OE	ENPWM5	ENPWM4

Mnemonic: PWMCON2 Address: CEh

BIT	NAME	FUNCTION
7~4	-	Reserved.
3	PWM5OE	Output enable for PWM5 0: Disable PWM5 Output. 1: Enable PWM5 Output.
2	PWM4OE	Output enable for PWM4 0: Disable PWM4 Output. 1: Enable PWM4 Output.
1	ENPWM5	Enable PWM5 0: Disable PWM5. 1: Enable PWM5.
0	ENPWM4	Enable PWM4 0: Disable PWM4. 1: Enable PWM4.

PWM 4 Register

Bit:	7	6	5	4	3	2	1	0
	PWM4.7	PWM4.6	PWM4.5	PWM4.4	PWM4.3	PWM4.2	PWM4.1	PWM4.0

Mnemonic: PWM 4 Address: CFh

Program Status Word

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set when an arithmetic operation results in a carry being generated from the ALU. It is also used as the accumulator for bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high-order nibble.
5	F0	User flag 0: A general-purpose flag that can be set or cleared by the user.
4	RS1	Register Bank select bits. See table below.
3	RS0	Register Bank select bits. See table below.
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the eighth bit, or vice versa, as a result of the previous operation.
1	F1	User flag 1: A general-purpose flag that can be set or cleared by the user.
0	P	Parity flag: Set and cleared by the hardware to indicate an odd or even number of 1's in the accumulator.

RS1, RS0: Register Bank select bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

Watchdog Control

Bit:	7	6	5	4	3	2	1	0
	-	POR	-	-	WDIF	WTRF	EWT	RWT

Mnemonic: WDCON Address: D8h

BIT	NAME	FUNCTION
7	-	Reserved.
6	POR	Power-on reset flag. The hardware sets this flag during power–up, and it can only be cleared by software. This flag can also be written by software.
5-4	-	Reserved.
3	WDIF	Watchdog Timer Interrupt Flag. If the watchdog interrupt is enabled, the hardware sets this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, this bit indicates that the time-out period has elapsed. This bit must be cleared by software.
2	WTRF	Watchdog Timer Reset Flag. If EWT is 0, the Watchdog Timer has no affect on this bit. Otherwise, the hardware sets this bit when the Watchdog Timer causes a reset. It can be cleared by software or a power-fail reset. It can be also read by software, which helps determine the cause of a reset.
1	EWT	Enable Watchdog-Timer Reset. Set this bit to enable the Watchdog Timer Reset function.
0	RWT	Reset Watchdog Timer. Set this bit to reset the Watchdog Timer before a time-out occurs. This bit is automatically cleared by the hardware.

The WDCON register is affected differently by different kinds of resets. After an external reset, the WDCON register is set to 0x0x0xx0b. After a Watchdog Timer reset, WTRF is set to 1, and the other bits are unaffected. On a power-on/-down reset, WTRF and EWT are set to 0, and POR is set to 1.

All the bits in this SFR have unrestricted read access. POR, EWT, WDIF and RWT are protected bits, so programs must follow the Timed Access procedure to write them. (See the TA Register description for more information.) This is illustrated in the following example.

```
TA      EG    C7H
WDCON   REG   D8H
CKCON   REG   8EH
        MOV   TA, #AAH
        MOV   TA, #55H
        SETB  WDCON.0              ; Reset Watchdog Timer
        ORL   CKCON, #11000000B    ; Select 26 bits Watchdog Timer
        MOV   TA, #AAH
        MOV   TA, #55H
        ORL   WDCON, #00000010B    ; Enable watchdog
```

The other bits in WDCON have unrestricted write access.

PWM Prescale Register

Bit:	7	6	5	4	3	2	1	0
	PWMP.7	PWMP.6	PWMP.5	PWMP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.0

Mnemonic: PWMP Address: D9h

PWM 0 Register

Bit:	7	6	5	4	3	2	1	0
	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0

Mnemonic: PWM0 Address: DAh

PWM 1 Register

Bit:	7	6	5	4	3	2	1	0
	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0

Mnemonic: PWM1 Address: DBh

PWM 0~3 Control Register 1

Bit:	7	6	5	4	3	2	1	0
	PWM3OE	PWM2OE	ENPWM3	ENPWM2	PWM1OE	PWM0OE	ENPWM1	ENPWM0

Mnemonic: PWMCON1 Address: DCh

BIT	NAME	FUNCTION
7	PWM3OE	Output enable for PWM3 0: Disable PWM3 Output. 1: Enable PWM3 Output.
6	PWM2OE	Output enable for PWM2 0: Disable PWM2 Output. 1: Enable PWM2 Output.
5	ENPWM3	Enable PWM3 0: Disable PWM3. 1: Enable PWM3.
4	ENPWM2	Enable PWM2 0: Disable PWM2. 1: Enable PWM2.
3	PWM1OE	Output enable for PWM1 0: Disable PWM1 Output. 1: Enable PWM1 Output.
2	PWM0OE	Output enable for PWM0 0: Disable PWM0 Output. 1: Enable PWM0 Output.
1	ENPWM1	Enable PWM1 0: Disable PWM1. 1: Enable PWM1.
0	ENPWM0	Enable PWM0 0: Disable PWM0. 1: Enable PWM0.

PWM 2 Register

Bit:	7	6	5	4	3	2	1	0
	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0

Mnemonic: PWM2 Address: DDh

PWM 3 Register

Bit:	7	6	5	4	3	2	1	0
	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0

Mnemonic: PWM3 Address: DEh

Accumulator

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

ACC.7-0: The A (or ACC) register is the standard 8051/52 accumulator.

ADC Control Register

Bit:	7	6	5	4	3	2	1	0
	ADC.1	ADC.0	ADCEX	ADCI	ADCS	AADR2	AADR1	AADR0

Mnemonic: ADCCON Address: E1h

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>7</td><td>ADC.1</td><td>Bit 1 of ADC result.</td></tr>
<tr><td>6</td><td>ADC.0</td><td>Bit 0 of ADC result.</td></tr>
<tr><td>5</td><td>ADCEX</td><td>Enable STADC-triggered conversion
0: Conversion can only be started by software (i.e., by setting ADCS).
1: Conversion can be started by software or by a rising edge on STADC (pin P2.0).</td></tr>
<tr><td>4</td><td>ADCI</td><td>ADC Interrupt flag: This flag is set when the result of an A/D conversion is ready. This generates an ADC interrupt, if it is enabled. The flag may be cleared by the ISR. While this flag is 1, the ADC cannot start a new conversion. ADCI can not be set by software.</td></tr>
<tr><td>3</td><td>ADCS</td><td>ADC Start and Status: Set this bit to start an A/D conversion. It may also be set by STADC if ADCEX is 1. This signal remains high while the ADC is busy and is reset right after ADCI is set. ADCS can not be reset by software, and the ADC cannot start a new conversion while ADCS is high.
<table>
<tr><th>ADCI</th><th>ADCS</th><th>ADC Status</th></tr>
<tr><td>0</td><td>0</td><td>ADC not busy; a conversion can be started</td></tr>
<tr><td>0</td><td>1</td><td>ADC busy; start of a new conversion is blocked</td></tr>
<tr><td>1</td><td>0</td><td>Conversion completed; start of a new conversion requires ADCI=0</td></tr>
<tr><td>1</td><td>1</td><td>Conversion completed; start of a new conversion requires ADCI=0</td></tr>
</table>
It is recommended to clear ADCI before ADCS is set. However, if ADCI is cleared and ADCS is set at the same time, a new A/D conversion may start on the same channel.</td></tr>
<tr><td>2</td><td>AADR2</td><td>See table below.</td></tr>
<tr><td>1</td><td>AADR1</td><td>See table below.</td></tr>
<tr><td>0</td><td>AADR0</td><td>See table below.</td></tr>
</table>

AADR2, AADR1, AADR0: ADC Analog Input Channel select bits:

These bits can only be changed when ADCI and ADCS are both zero.

AADR2	AADR1	AADR0	SELECTED ANALOG CHANNEL
0	0	0	ADC0
0	0	1	ADC1
0	1	0	ADC2
0	1	1	ADC3
1	0	0	ADC4
1	0	1	ADC5
1	1	0	ADC6
1	1	1	ADC7

ADC Conversion Result Register

Bit:	7	6	5	4	3	2	1	0
	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2

Mnemonic: ADCH Address: E2h

BIT	NAME	FUNCTION
7	ADC.9	Bit 9 of ADC result.
6	ADC.8	Bit 8 of ADC result.
5	ADC.7	Bit 7 of ADC result.
4	ADC.6	Bit 6 of ADC result.
3	ADC.5	Bit 5 of ADC result.
2	ADC.4	Bit 4 of ADC result.
1	ADC.3	Bit 3 of ADC result.
0	ADC.2	Bit 2 of ADC result.

ADC Conversion Enable Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	nADCEN

Mnemonic: ADCCEN Address: E4h

ADCCEN: Enable ADC Function.

1: Disables ADC analog circuit. (Default.)

0: Enable ADC analog circuit.

Extended Interrupt Enable

Bit:	7	6	5	4	3	2	1	0
	-	-	-	EWDI	-	-	-	-

Mnemonic: EIE Address: E8h

BIT	NAME	FUNCTION
7~5	-	Reserved. These bits read high
4	EWDI	Enable Watchdog Timer interrupt
3~0	-	Reserved. These bits read high

B Register

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B Address: F0h

B.7-0: The B register is the standard 8051/52 register that serves as a second accumulator.

Extended Interrupt Priority

Bit:	7	6	5	4	3	2	1	0
	-	-	-	PWDI	-	-	-	-

Mnemonic: EIP Address: F8h

BIT	NAME	FUNCTION
7~5	-	Reserved.
4	PWDI	Watchdog Timer Interrupt Priority. 1: High priority 0: Low priority
3~0	-	Reserved.

7. INSTRUCTION

The W79E201 executes all the instructions of the standard 8051/52 family. The operations of these instructions, as well as their effect on flag and status bits, are exactly the same. However, the timing of these instructions is different in two ways. First, the W79E201 machine cycle is four clock periods, while the standard-8051/52 machine cycle is twelve clock periods. Second, the W79E201 can fetch only once per machine cycle (i.e., four clocks per fetch), while the standard 8051/52 can twice per machine cycle (i.e., six clocks per fetch).

The timing difference creates an advantage for the W79E201. There is only one fetch per machine cycle, so the number of machine cycles is usually equal to the number of operands in the instruction. (Jumps and calls do require an additional cycle to calculate the new address.) As a result, the W79E201 reduces the number of dummy fetches and wasted cycles and improves overall efficiency, compared to the standard 8051/52.

7.1 Instruction Timing

This section is important because some applications use software instructions to generate timing delays. It also provides more information about timing differences between the W79E201 and the standard 8051/52.

In the W79E201, each machine cycle is four clock periods long. Each clock period is called a state, and each machine cycle consists of four states: C1, C2 C3 and C4, in order. Both clock edges are used for internal timing, so the duty cycle of the clock should be as close to 50% as possible.

The W79E201 does one op-code fetch per machine cycle, so, in most instructions, the number of machine cycles required is equal to the number of bytes in the instruction. There are 256 available op-codes. 128 of them are single-cycle instructions, so many op-codes are executed in just four clock periods. Some of the other op-codes are two-cycle instructions, and most of these have two-byte op-codes. However, there are some instructions that have one-byte instructions yet take two cycles to execute. One important example is the MOVX instruction.

In the standard 8051/52, the MOVX instruction is always two machine cycles long. However, in the W79E201, the duration of this instruction is controlled by the software. It can vary from two to nine machine cycles long, and the $\overline{RD}$ and $\overline{WR}$ strobe lines are elongated proportionally. This is called stretching, and it gives a lot of flexibility when accessing fast and slow peripherals. It also reduces the amount of external circuitry and software overhead.

The rest of the instructions are three-, four- or five-cycle instructions. At the end of this section, there are timing diagrams that provide an example of each type of instruction (single-cycle, two-cycle, …).

In summary, there are five types of instructions in the W79E201, based on the number of machine cycles, and each machine cycle is four clock periods long. The standard 8051/52 has only three types of instructions, based on the number of machine cycles, but each machine cycle is twelve clock periods long. As a result, even though the number of categories is higher, each instruction in the W79E201 runs 1.5 to 3 times faster, based on the number of clock periods, than it does in the standard 8051/52.

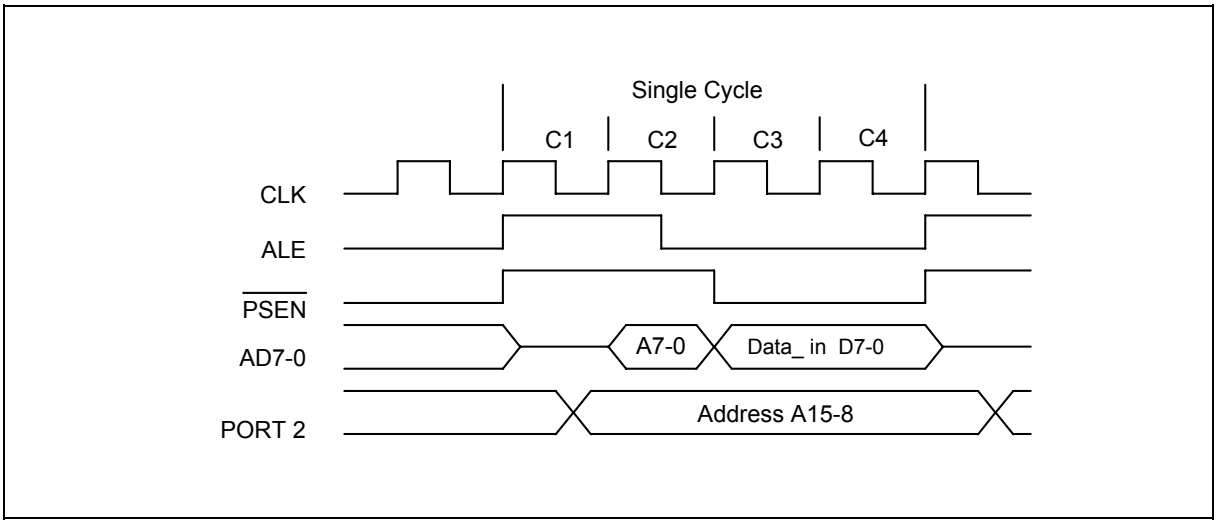


Figure 7-1 Single Cycle Instruction Timing

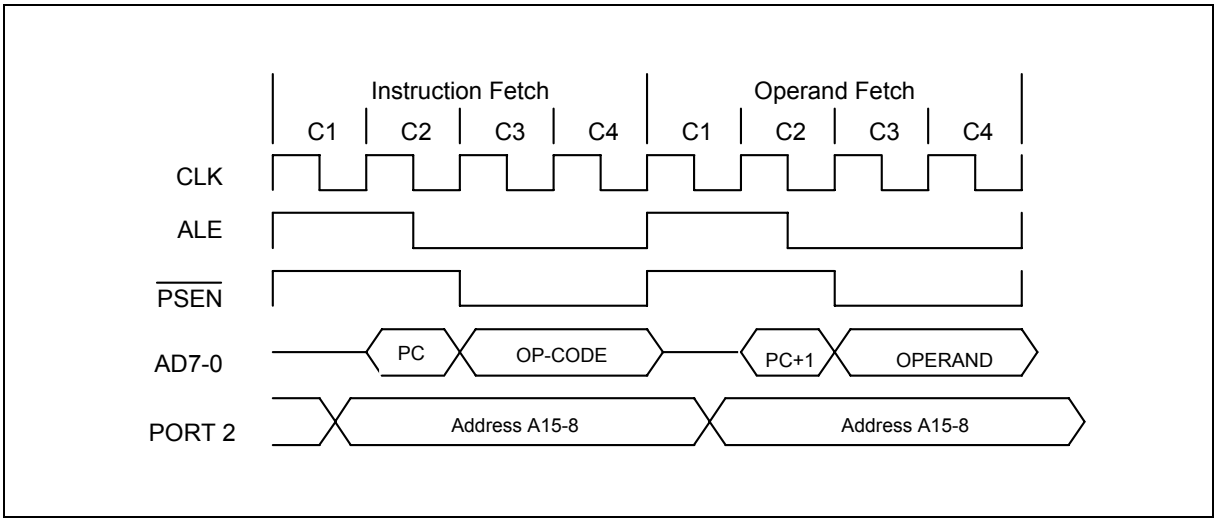


Figure 7-2 Two Cycle Instruction Timing

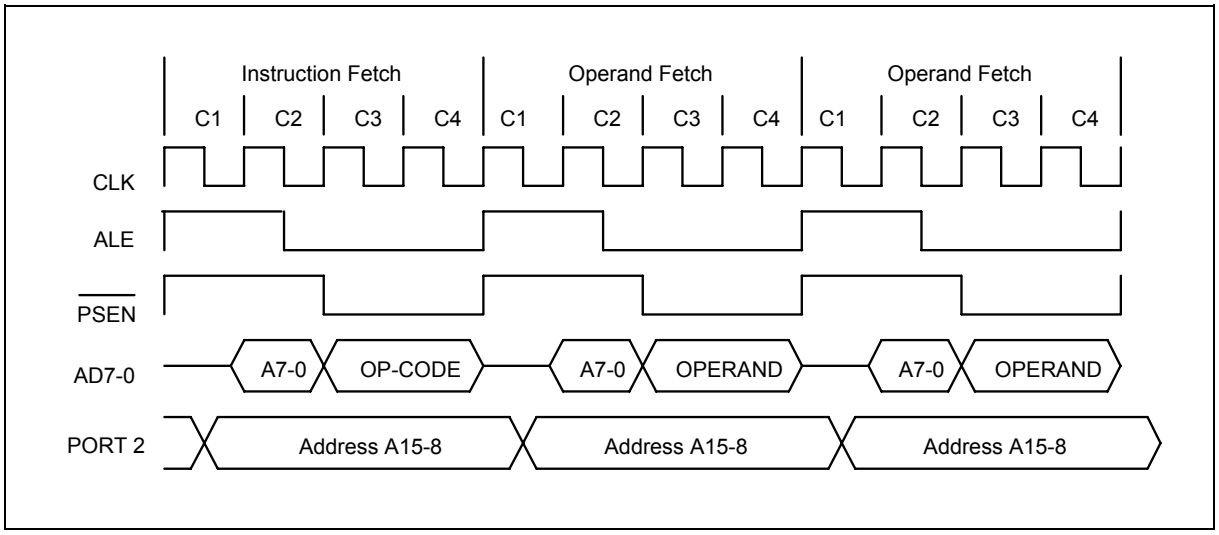


Figure 7-3 Three Cycle Instruction Timing

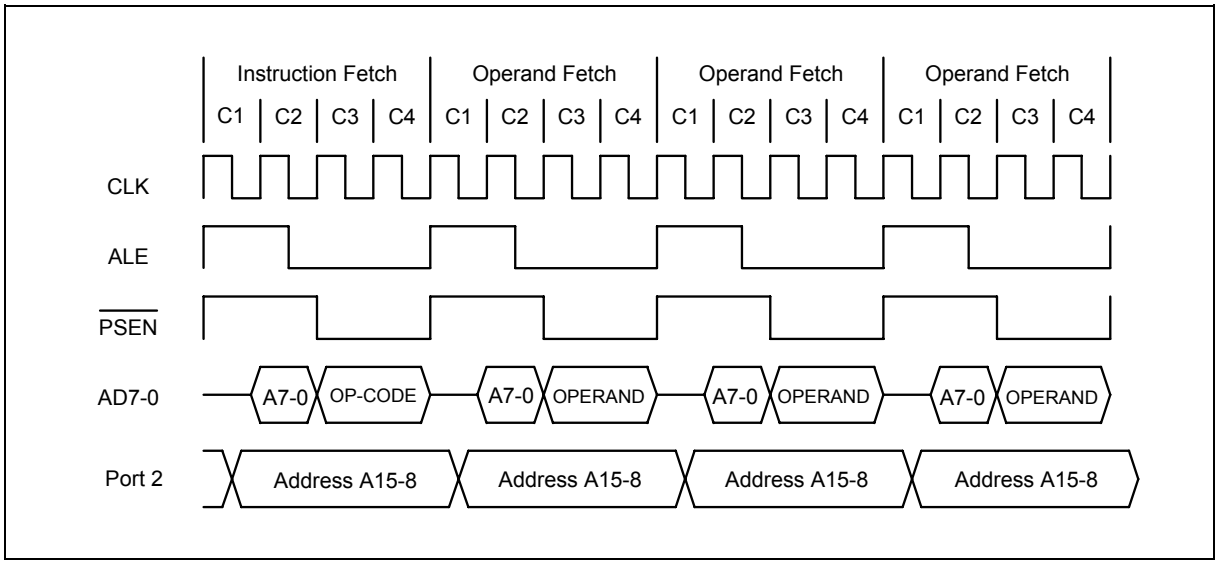


Figure 7-4 Four Cycle Instruction Timing

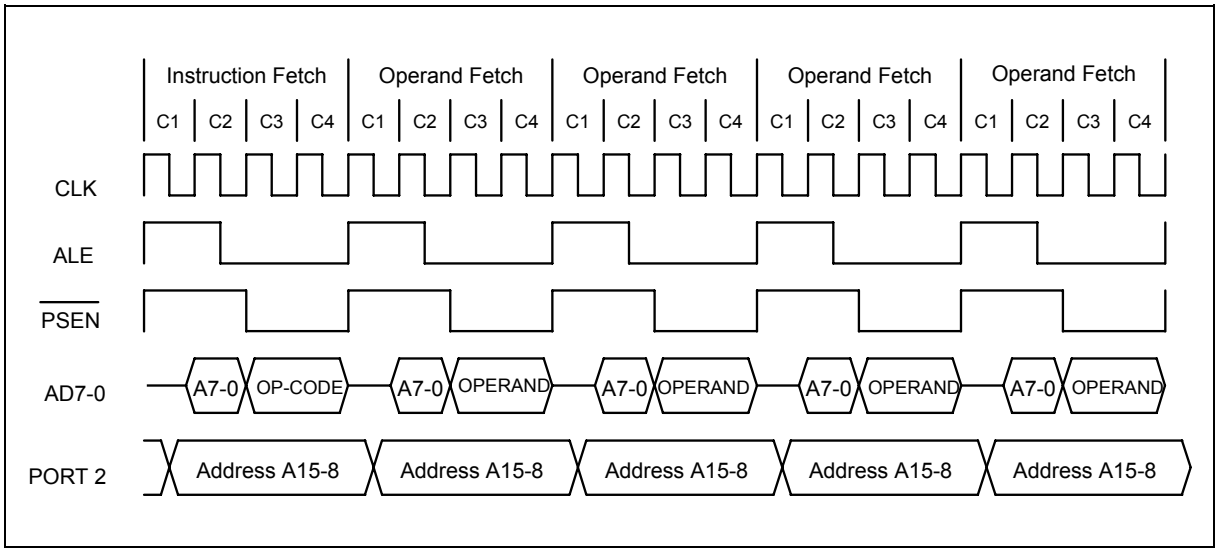


Figure 7-5 Five Cycle Instruction Timing

7.1.1 External Data Memory Access Timing

The timing for the MOVX instruction is another feature of the W79E201. In the standard 8051/52, the MOVX instruction has a fixed execution time of 2 machine cycles. However, in the W79E201, the duration of the access can be controlled by the user.

The instruction starts off as a normal op-code fetch that takes four clocks. In the next machine cycle, the W79E201 puts out the external memory address, and the actual access occurs. The user can control the duration of this access by setting the stretch value in CKCON, bits 2 – 0. As shown in the table below, these three bits can range from zero to seven, resulting in MOVX instructions that take two to nine machine cycles. The default value is one, resulting in a MOVX instruction of three machine cycles.

Table 2 Data Memory Cycle Stretch Values

M2	M1	M0	MACHINE CYCLES	$\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH IN CLOCKS
0	0	0	2	2
0	0	1	3 **(default)**	4
0	1	0	4	8
0	1	1	5	12
1	0	0	6	16
1	0	1	7	20
1	1	0	8	24
1	1	1	9	28

Stretching only affects the MOVX instruction. There is no effect on any other instruction or its timing, it is as if the state of the CPU is held for the desired period. The timing waveforms when the stretch value is zero, one, and two are shown below.

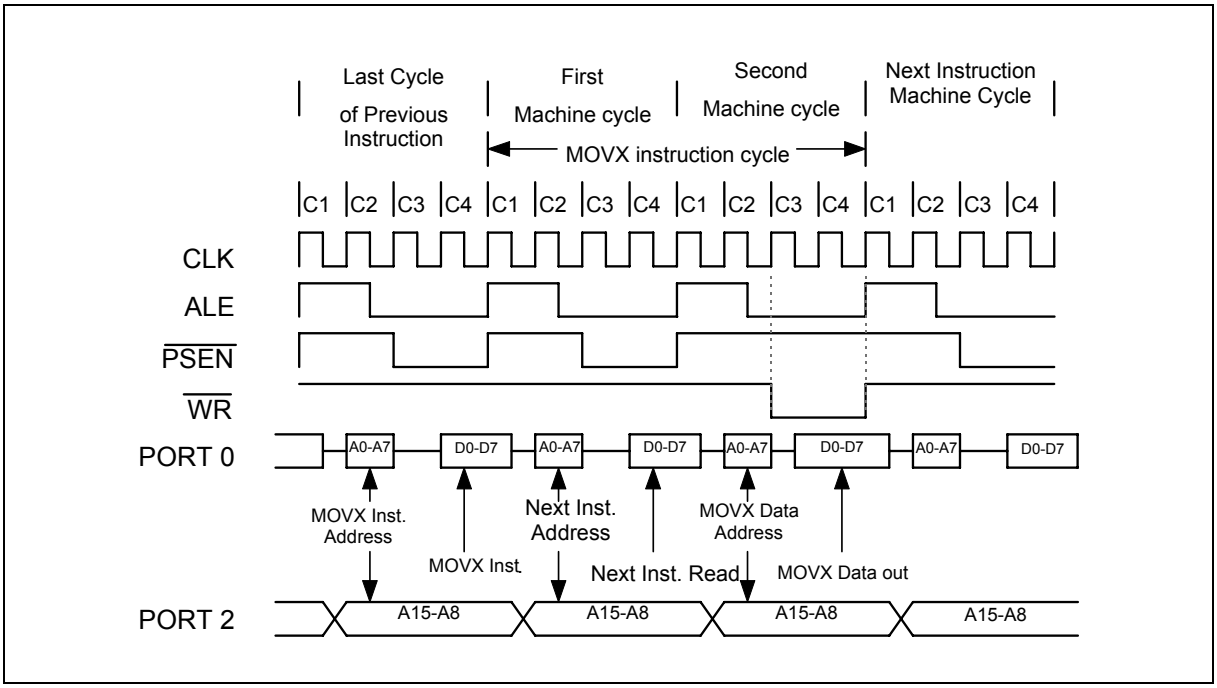


Figure 7-6 Data Memory Write with Stretch Value = 0

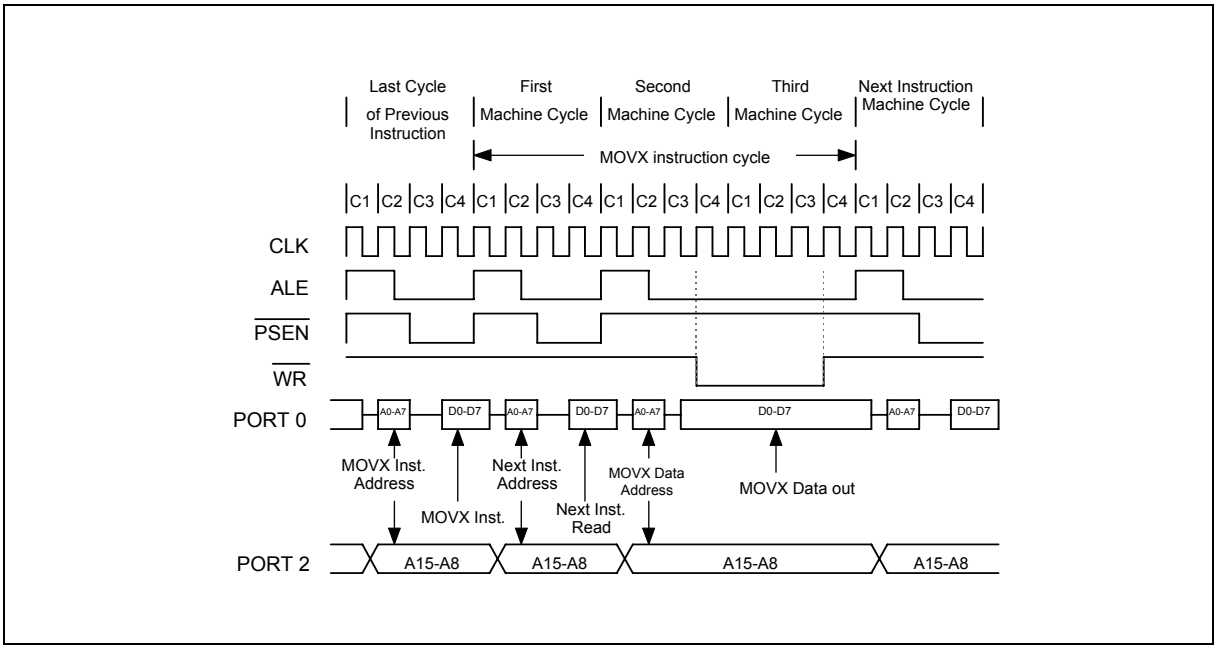


Figure 7-7 Data Memory Write with Stretch Value = 1

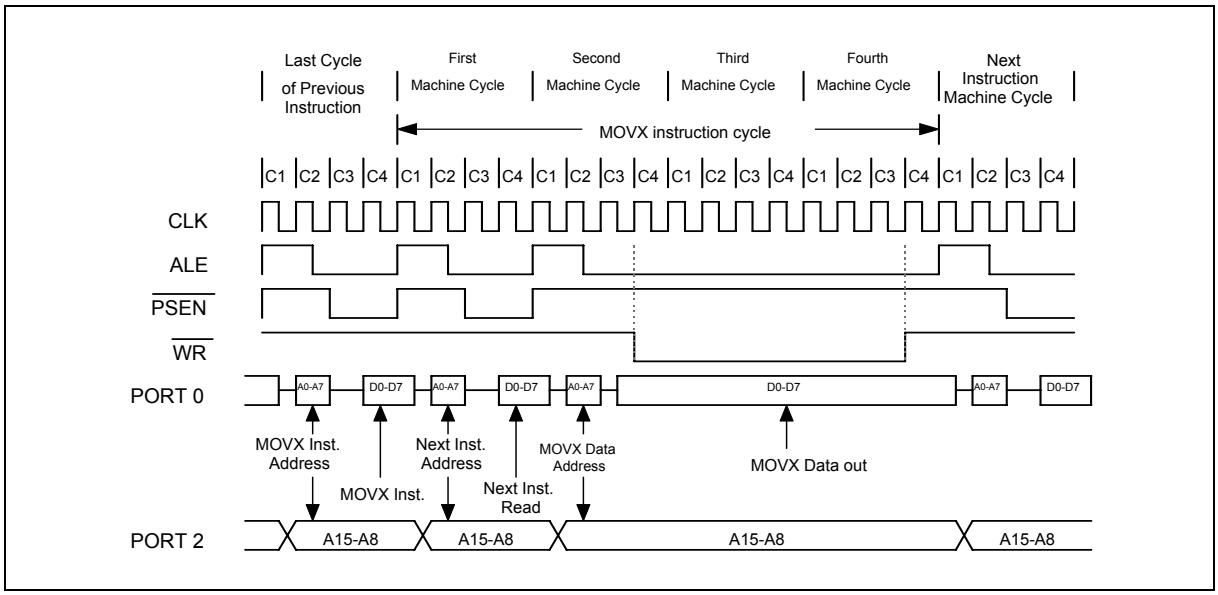


Figure 7-8 Data Memory Write with Stretch Value = 2

8. POWER MANAGEMENT

The W79E201 provides idle mode and power-down mode to control power consumption. These modes are discussed in the next two sections, followed by a discussion of resets.

8.1 Idle Mode

Write a one to PCON, bit 0, to put the device in Idle mode. The instruction that sets the idle bit is the last instruction executed before the device goes into Idle mode. In Idle mode, the clock to the CPU is halted, but not the one to the Interrupt, Timer, Watchdog Timer and Serial Port. This freezes the CPU state, including the Program Counter, Stack Pointer, Program Status Word, Accumulator and registers. The ALE and PSEN pins are held high, and port pins hold the same states they had when the device went into Idle mode. Table 3 below provides the values of various pins in Idle mode.

Idle mode can be terminated two ways. First, since the interrupt controller is still active, any enabled interrupt wakes up the processor. This automatically clears the Idle bit, terminates Idle mode, and executes the Interrupt Service Routine (ISR). After the ISR, the program resumes after the instruction that put the device into Idle mode.

Idle mode can also be exited by a reset, such as a high signal on the external RST pin, a power-on reset or a Watchdog Timer reset (if enabled). During reset, the program counter is reset to 0000h, so the instruction following the one that put the device into Idle mode is not executed. All the SFRs are also reset to their default values. Since the clock is already running, there is no delay, and execution starts immediately.

8.2 Power Down Mode

Write a one to PCON, bit 1, to put the device in Power-Down mode. The instruction that sets the power-down bit is the last instruction executed before the device goes into Power-Down mode. In Power-Down mode, all the clocks and all activity stop completely, and power consumption is reduced to the lowest possible value. The ALE and $\overline{\text{PSEN}}$ pins are pulled low, and port pins output the values held by their respective registers. Table 3 provides the values of various pins in Power-Down mode.

The W79E201 can exit Power-Down mode two ways. First, it can be exited by a reset, such as a high signal on the external RST pin or a power-on reset. The Watchdog Timer cannot provide a reset to exit Power-Down mode because the clock has stopped. A reset terminates Power-Down mode, restarts the clock, and restarts program execution at 0000h.

The W79E201 can also exit Power-Down mode by an external interrupt pin, as long as the external input has been set to level-detect, the corresponding interrupt is enabled, and the global enable (EA) bit is set. If these conditions are met, then a low-level signal on the external pin re-starts the oscillator. The device executes the interrupt service routine (ISR) for the corresponding external interrupt, and, afterwards, the program resumes execution after the one that put the device into Power-Down mode.

Table 3 Status of External Pins in Idle and Power-Down Mode

MODE	PROGRAM MEMORY	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

8.3 Reset Conditions

There are three ways to reset the W79E201—External Reset, Watchdog Timer Reset and Power-On Reset. In general, most registers return to their default values regardless of the source of the reset, but a couple flags depend on the source. As a result, the user can use these flags to determine the cause of the reset.

The rest of this section discusses the three causes of resets and then elaborates on the reset state.

8.3.1 External Reset

The device samples the RST pin every machine cycle during state C4. The RST pin must be held high for at least two machine cycles before the reset circuitry applies an internal reset signal. Thus, this reset is a synchronous operation and requires the clock to be running.

The device remains in the reset state as long as RST is one and remains there up to two machine cycles after RST is deactivated. Then, the device begins program execution at 0000h. There are no flags associated with the external reset, but, since the other two reset sources do have flags, the external reset is the cause if those flags are clear.

8.3.2 Power-On Reset (POR)

If the power supply falls below V_{rst}, the device goes into the reset state. When the power supply returns to proper levels, the device performs a power-on reset and sets the POR flag. The software should clear the POR flag, or it will be difficult to determine the source of future resets.

8.3.3 Watchdog Timer Reset

The Watchdog Timer is a free-running timer with programmable time-out intervals. The program must clear the Watchdog Timer before the time-out interval is reached to restart the count. If the time-out interval is reached, an interrupt flag is set. 512 clocks later, if the Watchdog Reset is enabled and the Watchdog Timer has not been cleared, the Watchdog Timer generates a reset. The reset condition is maintained by the hardware for two machine cycles, and the WTRF bit in WDCON is set. Afterwards, the device begins program execution at 0000h.

Reset State

When the device is reset, most registers return to their initial state. The Watchdog Timer is disabled if the reset source was a power-on reset. The port registers are set to FFh, which puts most of the port pins in a high state and makes Port 0 float (as it does not have on-chip pull-up resistors). The Program Counter is set to 0000h, and the stack pointer is reset to 07h. After this, the device remains in the reset state as long as the reset conditions are satisfied. Table 4 provides the reset values for every SFR.

Table 4 SFR Reset Value

SFR NAME	RESET VALUE	SFR NAME	RESET VALUE
P0	11111111b	EIP	xxx00000b
SP	00000111b	IP	x0000000b
DPL	00000000b	SADEN	00000000b
DPH	00000000b	PMR	xxxxx0xxb
PCON	00xx0000b	STATUT2	000x0000b
TCON	00000000b	T2CON	00000000b
TMOD	00000000b	T2MOD	00000x00b

Table 4 SFR Reset Value, continued

SFR NAME	RESET VALUE	SFR NAME	RESET VALUE
TL0	00000000b	RCAP2L	00000000b
TL1	00000000b	RCAP2H	00000000b
TH0	00000000b	TL2	00000000b
TH1	00000000b	TH2	00000000b
CKCON	00000001b	PSW	00000000b
P1	11111111b	WDCON	see below
SCON	00000000b	PWMP	00000000b
SBUF	xxxxxxxxb	PWMCON1	00000000b
P2	11111111b	PWM0	00000000b
P0R	00000000b	PWM1	00000000b
P4	Xxxxxxx1b	PWM2	00000000b
IE	00000000b	PWM3	00000000b
SADDR	00000000b	ACC	00000000b
CHPCON	00000000b	ADCCON	xxxxx000b
SFRAL	00000000b	ADCH	xxxxxxxxb
SFRAH	00000000b	ADCCEN	xxxxxxx1b
SFRFD	11111111b	PWMCON2	00000000b
SFRCN	00111111b	PWM4	00000000b
P3	11111111b	EIE	xxx00000b
PWM5	00000000b	B	00000000b

The WDCON register reset value depends on the source of the reset.

	External reset	Watchdog reset	Power on reset
WDCON	0x0x0xx0b	0x0x01x0b	01000000b

The WTRF bit is set by a Watchdog Timer reset, and the POR bit is set by a power-on reset. A power-on reset also clears the WTRF and EWT bits, which clears the Watchdog Timer reset flag and disables the Watchdog Timer. In contrast, the Watchdog Timer reset and External reset have no effect on the EWT bit.

Reset does not affect the on-chip RAM, however, so RAM is preserved as long as V_{DD} remains above approximately 2 V, the minimum operating voltage for the RAM. If V_{DD} falls below 2 V, the RAM contents are also lost. In either case, the stack pointer is always reset, so the stack contents are lost.

9. INTERRUPTS

The W79E201 has eight interrupt sources and a two-level priority structure. Each interrupt source has a separate priority bit, interrupt flag, interrupt enable bit, and interrupt vector. In addition, W79E201 interrupts can be globally disabled. This section discusses the interrupt sources and the two-level priority structure.

External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can be edge-triggered or level-triggered, depending on bits IT0 and IT1. In edge-triggered mode, the INTx input is sampled every machine cycle. If the sample is high in one cycle and low in the next, then a high-to-low transition is detected, and the interrupt request flag IEx in TCON is set. This flag requests the interrupt, and it is automatically cleared when the interrupt service routine is called. Since external interrupts are sampled every machine cycle, the input has to be held high or low for at least one complete machine cycle. In level-triggered mode, the requesting source has to hold the pin low until the interrupt is serviced. The IEx flag is not cleared automatically when the service routine is called, and, if the input continues to be held low after the service routine is completed, the signal may generate another interrupt request.

Timer 0 and 1 interrupts are generated by the TF0 and TF1 flags. These flags are set by a timer overflow, and they are cleared automatically when the interrupt service routine is called. The Timer 2 interrupt is generated by a logical-OR of the TF2 (overflow) and the EXF2 (capture / reload events) flags. The hardware does not clear these flags when the interrupt service routine is called, so the software has to resolve the cause of the interrupt and clear the appropriate flag(s).

The Watchdog Timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog Timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by bit EIE.4, then an interrupt is generated.

All of the interrupt flags can be set or reset by software, as well as hardware, by setting or clearing the appropriate bit in the IE register. This register also has the global disable bit EA, which can be cleared to disable all interrupts.

There are two priority levels for interrupts, high and low, and the priority of each interrupt source can be set individually. When two interrupts have the same priority, there is a pre-defined hierarchy to resolve simultaneous requests. This hierarchy is shown below, highest-priority interrupts first.

Table 5 Priority structure of interrupts

SOURCE	FLAG	VECTOR ADDRESS	PRIORITY LEVEL
External Interrupt 0	IE0	0003h	1(highest)
ADC Interrupt	ADCI	006Bh	2
Timer 0 Overflow	TF0	000Bh	3
External Interrupt 1	IE1	0013h	4
Timer 1 Overflow	TF1	001Bh	5
Serial Port	RI + TI	0023h	6
Timer 2 Overflow	TF2 + EXF2	002Bh	7
Watchdog Timer	WDIF	0063h	8 (lowest)

10. PROGRAMMABLE TIMERS/COUNTERS

The W79E201 has three 16-bit programmable timer/counters and one programmable Watchdog Timer. This section discusses Timer/Counters 0 and 1, Timer/Counter 2, and the Watchdog Timer separately.

10.1 Timer/Counters 0 and 1

Timer/Counters 0 and 1 are each 16-bit timer/counters, composed of two separate, 8-bit registers. Timer/Counter 0 is composed of TH0 (the 8 MSB) and TL0 (the 8 LSB), while Timer/Counter 1 is composed of TH1 and TL1. Timer/Counters 0 and 1 operate in one of four modes as timers, machine-cycle counters or external-input counters. The timer or counter function is selected by the "$C/\overline{T}$" bit in TMOD, and the mode is selected by bits M0 and M1 in TMOD. Each timer/counter can be configured separately.

In timer and counter modes, the count register is updated at C3. When configured as a timer, the timer/counter counts clock cycles, and the timer clock can be 1/12 or 1/4 of the system clock. In counter mode, the register increments on the falling edge of the corresponding external input pin, T0 for Timer 0 and T1 for Timer 1. T0 and T1 are sampled every machine cycle at C4. If the sampled value is high one machine cycle and low the next, a valid high-to-low transition is recognized, and the count register is incremented in the following machine cycle at C3. Since it takes two machine cycles to recognize a falling edge, counting takes place no faster than 1/24 of the master clock frequency.

The rest of this section explains time-base selection and then introduces the four operating modes.

10.1.1 Time-Base Selection

The W79E201 can operate like the standard 8051/52 family, counting at the rate of 1/12 of the clock speed, or in turbo mode, counting at the rate of 1/4 clock speed. The speed is controlled by the T0M and T1M bits in CKCON, and the default value is zero, which uses the standard 8051/52 speed.

Mode 0

In Mode 0, the timer/counter is a 13-bit counter. The 13-bit counter consists of THx (8 MSB) and the five lower bits of TLx (5 LSB). The upper three bits of TLx are ignored. The timer/counter is enabled when TRx is set and either GATE is 0 or $\overline{INTx}$ is 1. When $C/\overline{T}$ is 0, the timer/counter counts clock cycles; when $C/\overline{T}$ is 1, it counts falling edges on T0 (P3.4 for Timer 0) or T1 (P3.5 for Timer 1). For clock cycles, the time base may be 1/12 or 1/4 clock speed, and the falling edge of the clock increments the counter. When the 13-bit value moves from 1FFFh to 0000h, the timer overflow flag TFx is set, and an interrupt occurs if enabled. This is illustrated below.

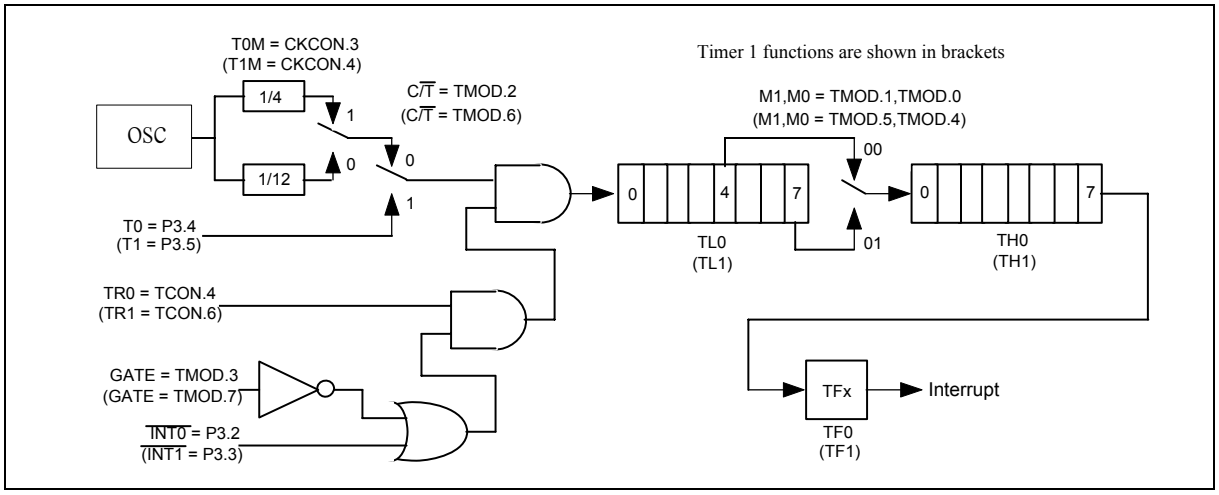


Figure 10-1 Timer/Counter Mode 0 & Mode 1

Mode 1

Mode 1 is the same as Mode 0, except that the timer/counter is 16 bits, instead of 13 bits.

Mode 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as a 8 bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{\text{INTx}}$ pins. As in the other two modes 0 and 1 mode 2 allows counting of either clock cycles (clock/12 or clock/4) or pulses on pin Tn.

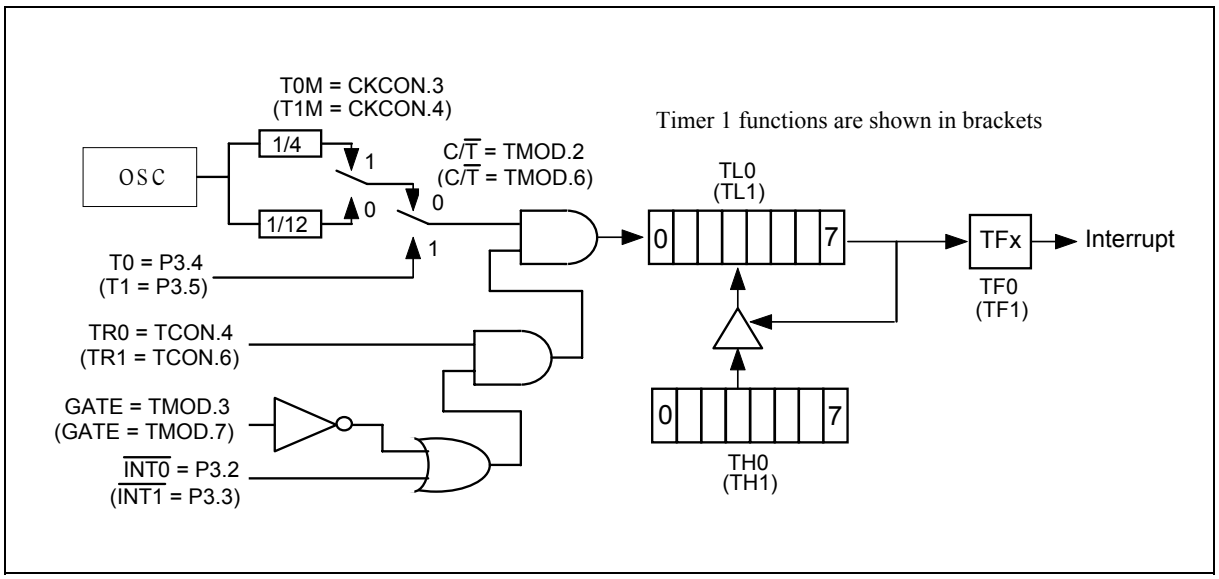


Figure 10-2 Timer/Counter Mode 2

Mode 3

Mode 3 is used when an extra 8-bit timer is needed. It has a different effect on Timer 0 and Timer 1. TL0 and TH0 become two separate 8 bit counters. TL0 uses the Timer 0 control bits C/$\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0, and it can be used to count clock cycles (clock/12 or clock/4) or falling edges on pin T0, as determined by C/$\overline{T}$ (TMOD.2). TH0 becomes a clock-cycle counter (clock/12 or clock/4) and takes over the Timer 1 enable bit TR1 and overflow flag TF1. In contrast, mode 3 simply freezes Timer 1. If Timer 0 is in mode 3, Timer 1 can still be used in modes 0, 1 and 2, but it no longer has control over TR1 and TF1. It can also be used as a baud-rate generator for the serial port.

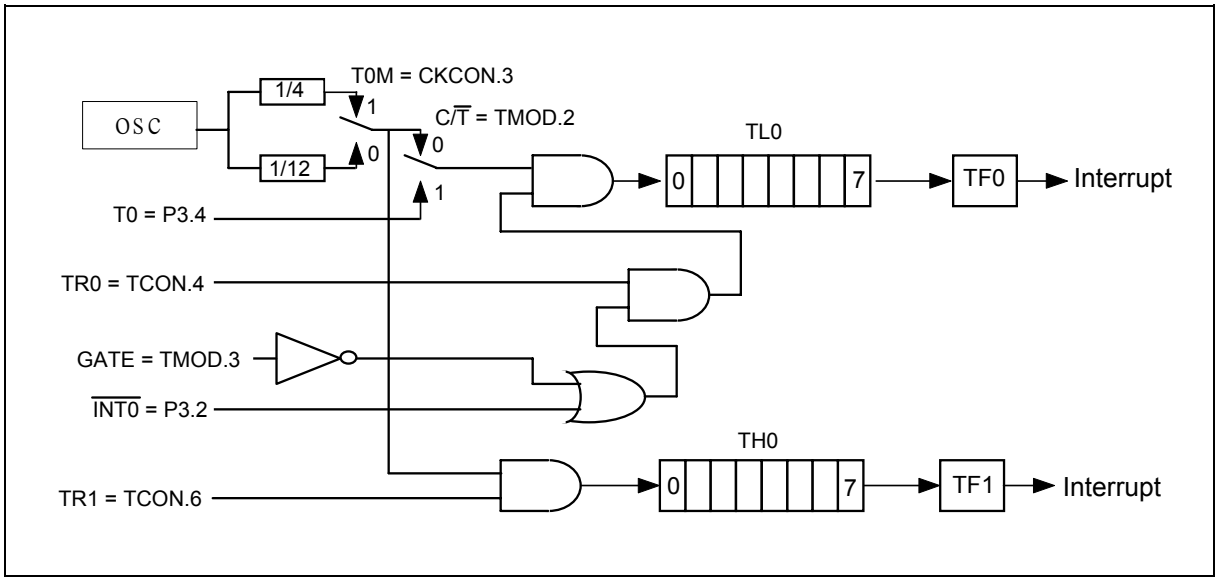


Figure 10-3 Timer/Counter 0 Mode 3

10.2 Timer/Counter 2

Timer/Counter 2 is a 16-bit up/down-counter equipped with a capture/reload capability. The clock source for Timer/Counter 2 may be the external T2 pin (C/$\overline{T2}$ = 1) or the crystal oscillator (C/$\overline{T2}$ = 0), divided by 12 or 4. The clock is enabled and disabled by TR2. Timer/Counter 2 runs in one of four operating modes, each of which is discussed below.

10.2.1 Capture Mode

Capture mode is enabled by setting CP/$\overline{RL2}$ in T2CON to 1. In capture mode, Timer/Counter 2 is a 16-bit up-counter. When the counter rolls over from FFFFh to 0000h, the timer overflow flag TF2 is set, and an interrupt is generated, if enabled.

If the EXEN2 bit is set, a negative transition on the T2EX pin captures the current value of TL2 and TH2 in the RCAP2L and RCAP2H registers. It also sets the EXF2 bit in T2CON, which generates an interrupt if enabled. In addition, if the T2CR bit in T2MOD is set, the W79E201 resets Timer 2 automatically after the capture. This is illustrated below.

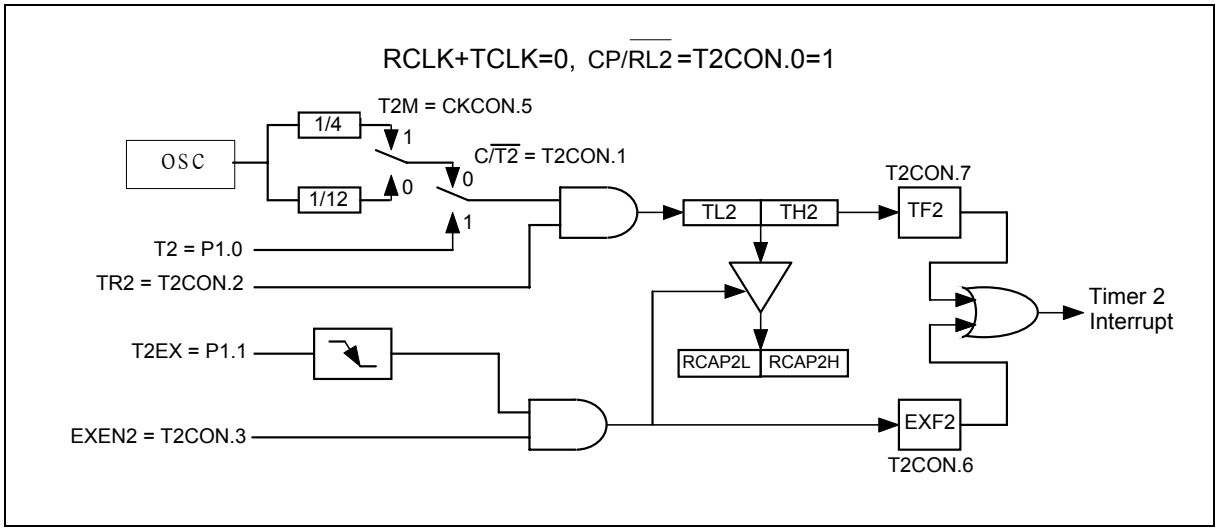


Figure 10-4 16-Bit Capture Mode

10.2.2 Auto-Reload Mode, Counting Up

This mode is enabled by clearing CP/RL2 in T2CON register and DCEN in T2MOD. In this mode, Timer/Counter 2 is a 16-bit up-counter. When the counter rolls over from FFFFh to 0000h, the timer overflow flag TF2 is set, and TL2 and TH2 capture the contents of RCAP2L and RCAP2H, respectively. Alternatively, if EXEN2 is set, a negative transition on the T2EX pin causes a reload, which also sets the EXF2 bit in T2CON.

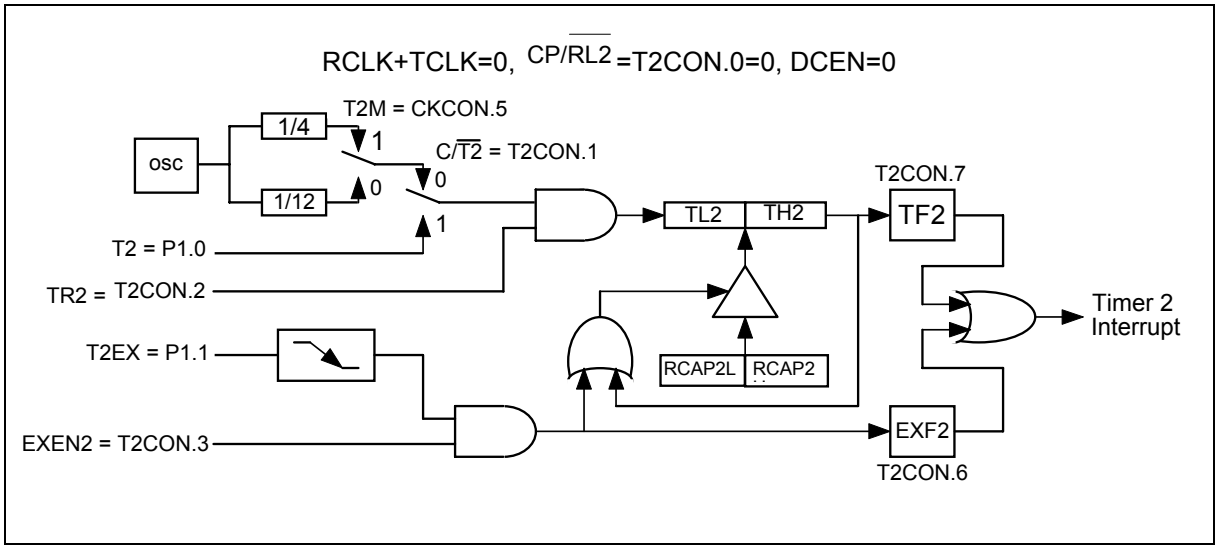


Figure 10-5 16-Bit Auto-reload Mode, Counting Up

10.2.3 Auto-Reload Mode, Counting Up/Down

This mode is enabled by clearing CP/$\overline{RL2}$ in T2CON and setting DCEN in T2MOD. In this mode, Timer/Counter 2 is a 16-bit up/down-counter, whose direction is controlled by the T2EX pin (1 = up, 0 = down). If Timer/Counter 2 is counting up, an overflow reloads TL2 and TH2 with the contents of the capture registers RCAP2L and RCAP2H. If Timer/Counter 2 is counting down, TL2 and TH2 are loaded with FFFFh when the contents of Timer/Counter 2 equal the capture registers RCAP2L and RCAP2H. Regardless of direction, reloading sets the TF2 bit. It also toggles the EXF2 bit, but the EXF2 bit can not generate an interrupt in this mode. This is illustrated below.

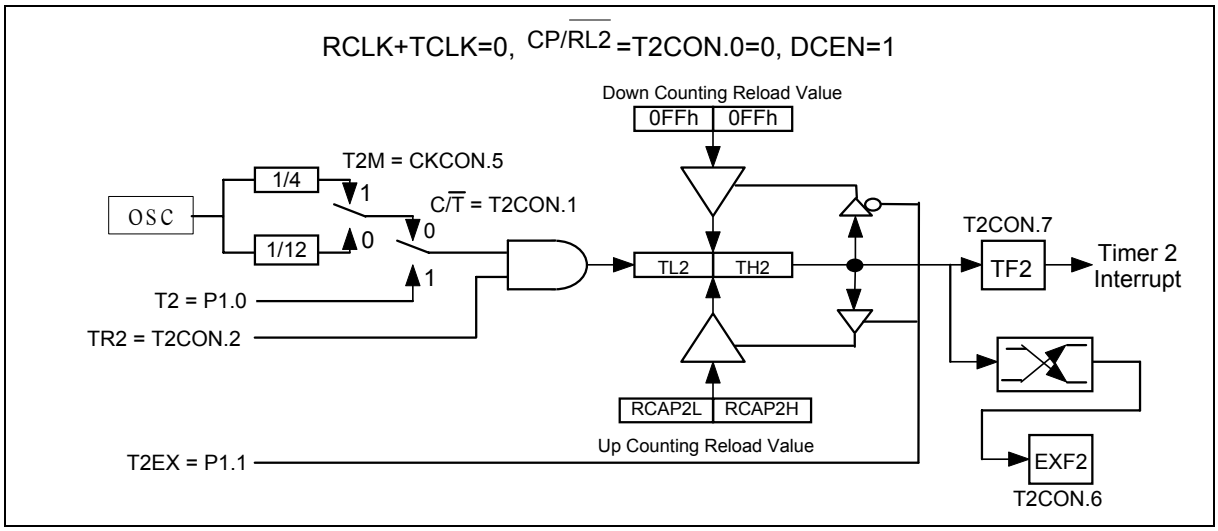


Figure 10-6 16-Bit Auto-reload Up/Down Counter

10.2.4 Baud Rate Generator Mode

Baud rate generator mode is enabled by setting either RCLK or TCLK in T2CON. In baud rate generator mode, Timer/Counter 2 is a 16-bit counter with auto-reload when the count rolls over from FFFFh. However, rolling-over does not set TF2. If EXEN2 is set, then a negative transition on the T2EX pin sets EXF2 bit in the T2CON register and causes an interrupt request.

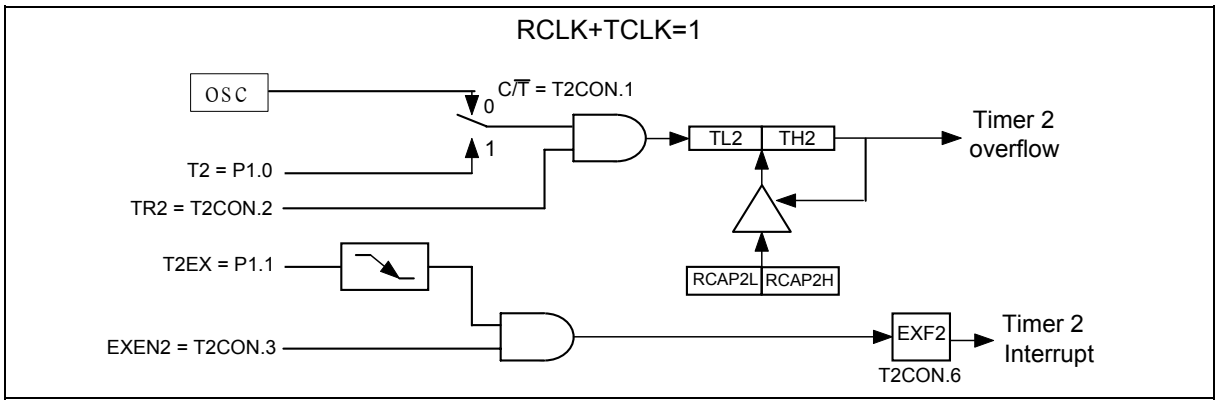


Figure 10-7 Baud Rate Generator Mode

11. WATCHDOG TIMER

The Watchdog Timer is a free-running timer that can be programmed to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock to determine the time-out interval. When the time-out occurs, a flag is set, which can generate an interrupt or a system reset, if enabled. The interrupt occurs if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together.

The main use of the Watchdog Timer is as a system monitor. In case of power glitches or electromagnetic interference, the processor may begin to execute errant code. The Watchdog Timer helps the W79E201 recover from these states. During development, the code is first written without the watchdog interrupt or reset. Then, the watchdog interrupt is enabled to identify code locations where the interrupt occurs, and instructions are inserted to reset the Watchdog Timer in these locations. In the final version, the watchdog interrupt is disabled, and the watchdog reset is enabled. If errant code is executed, the Watchdog Timer is not reset at the required times, so a Watchdog Timer reset occurs.

When used as a simple timer, the reset and interrupt functions are disabled. The Watchdog Timer can be started by RWT and sets the WDIF flag after the selected time interval. Meanwhile, the program polls the WDIF flag to find out when the selected time interval has passed. Alternatively, the Watchdog Timer can also be used as a very long timer. In this case, the interrupt feature is enabled.

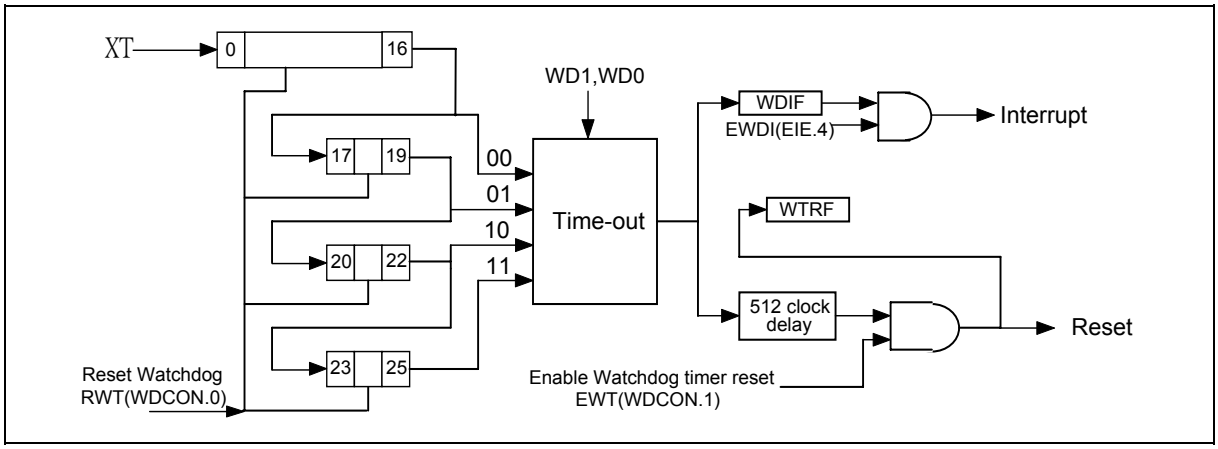


Figure 11-1 Watchdog Timer

The Watchdog Timer should be started by RWT because this ensures that the timer starts from a known state. The RWT bit is self-clearing; i.e., after writing a 1 to this bit, the bit is automatically cleared. After setting RWT, the Watchdog Timer begins counting clock cycles. The time-out interval is selected by WD1 and WD0 (CKCON.7 and CKCON.6).

Table 6 Time-out values for the Watchdog Timer

WD1	WD0	WATCHDOG INTERVAL	NUMBER OF CLOCKS	TIME @ 1.8432 MHZ	TIME @ 10 MHZ
0	0	2^{17}	131072	71.11 ms	13.11 ms
0	1	2^{20}	1048576	568.89 ms	104.86 ms
1	0	2^{23}	8388608	4551.11 ms	838.86 ms
1	1	2^{26}	67108864	36408.88 ms	6710.89 ms

When the selected time-out occurs, the watchdog interrupt flag WDIF (WDCON.3) is set. Then, if there is no RWT and if the Watchdog Timer reset EWT (WDCON.1) is enabled, the Watchdog Timer reset occurs 512 clocks later. This reset lasts two machine cycles, and the Watchdog Timer reset flag WTRF (WDCON.2) is set, which indicates that the Watchdog Timer caused the reset.

The Watchdog Timer is disabled by a power-on/fail reset. The external reset and Watchdog Timer reset can not disable Watchdog Timer but restart the Timer.

The control bits that support the Watchdog Timer are discussed below.

Watchdog Timer Control

BIT	NAME	FUNCTION
7	-	Reserved.
6	POR	Power-on reset flag. Hardware will set this flag on a power up condition. This flag can be read or written by software. A write by software is the only way to clear this bit once it is set.
5	-	Reserved.
4	-	Reserved.
3	WDIF	Watchdog Timer Interrupt Flag. If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software.
2	WTRF	Watchdog Timer Reset Flag. Hardware will set this bit when the Watchdog Timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWT = 0, the Watchdog Timer will have no affect on this bit.
1	EWT	Enable Watchdog Timer Reset. Setting this bit will enable the Watchdog Timer Reset function.
0	RWT	Reset Watchdog Timer. This bit helps in putting the Watchdog Timer into a know state. It also helps in resetting the Watchdog Timer before a time-out occurs. Failing to set the EWT before time-out will cause an interrupt, if EWDI (EIE.4) is set, and 512 clocks after that a Watchdog Timer reset will be generated if EWT is set. This bit is self-clearing by hardware.

The EWT, WDIF and RWT bits are protected by the Timed Access procedure. This procedure prevents software, especially errant code, from accidentally enabling or disabling the Watchdog Timer. An example is provided below.

```
        org     63h
        mov     TA,#AAH
        mov     TA,#55H
        clr     WDIF
        jnb     execute_reset_flag,bypass_reset     ; Test if CPU need to reset.
        jmp     $                                   ; Wait to reset
bypass_reset:
        mov     TA,#AAH
        mov     TA,#55H
        setb    RWT
        reti

        org     300h
start:
        mov     ckcon,#01h      ; select 2 ^ 17 timer
;       mov     ckcon,#61h      ; select 2 ^ 20 timer
;       mov     ckcon,#81h      ; select 2 ^ 23 timer
;       mov     ckcon,#c1h      ; select 2 ^ 26 timer
        mov     TA,#aah
        mov     TA,#55h
        mov     WDCON,#00000011B
        setb    EWDI
        setb    ea
        jmp     $               ; wait time out
```

Clock Control

WD1, WD0: CKCON.7, CKCON.6 - Watchdog Timer Mode select bits. These two bits select the time-out interval for the Watchdog Timer. The reset interval is 512 clocks longer than the selected interval. The default time-out is 2^{17} clocks, the shortest time-out period.

12. SERIAL PORT

The W79E201 serial port is a full-duplex port, and the W79E201 provides additional features, such as Frame Error Detection and Automatic Address Recognition. The serial port is capable of synchronous and asynchronous communication. In synchronous mode, the W79E201 generates the clock and operates in half-duplex mode. In asynchronous mode, the serial port can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF, but any write to SBUF writes to the transmit register while any read from SBUF reads from the receive buffer. The serial port can operate in four modes, as described below.

12.1 Mode 0

This mode provides half-duplex, synchronous communication with external devices. In this mode, serial data is transmitted and received on the RXD line, and the W79E201 provides the shift clock on TxD, whether the device is transmitting or receiving. Eight bits are transmitted or received per frame, LSB first. The baud rate is 1/12 or 1/4 of the oscillator frequency, as determined by the SM2 bit (SCON.5; 0 = 1/12; 1 = 1/4). This programmable baud rate is the only difference between the standard 8051/52 and the W79E201 in mode 0.

Any write to SBUF starts transmission. The shift clock is activated, and data is shifted out on RxD until all eight bits are transmitted. If SM2 is 1, the data appears on RxD one clock period before the falling edge of the shift clock on TxD. Then, the clock remains low for two clock periods before going high again. If SM2 is 0, the data appears on RxD three clock periods before the falling edge of the shift clock on TxD, and the clock on TxD remains low for six clock periods before going high again. This ensures that, at the receiving end, the data on the RxD line can be clocked on the rising edge of the shift clock or latched when the clock is low. The TI flag is set high in C1 following the end of transmission. The functional block diagram is shown below.

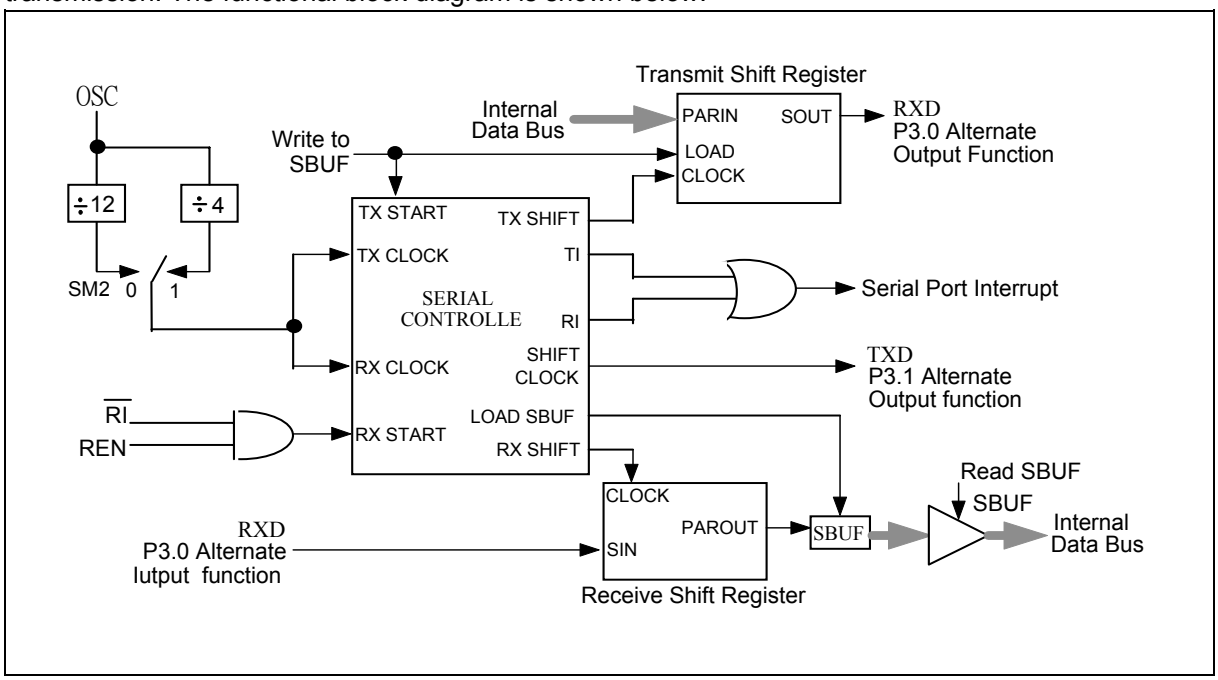


Figure 12-1 Serial Port Mode 0

The serial port receives data when REN is 1 and RI is zero. The shift clock (TxD) is activated, and the serial port latches data on the rising edge of the shift clock. The external device should, therefore, present data on the falling edge of the shift clock. This process continues until all eight bits have been received. The RI flag is set in C1 following the last rising edge of the shift clock, which stops reception until RI is cleared by the software.

12.2 Mode 1

In Mode 1, full-duplex asynchronous communication is used. Frames consist of ten bits transmitted on TXD and received on RXD. The ten bits consist of a start bit (0), eight data bits (LSB first), and a stop bit (1). When receiving, the stop bit goes into RB8 in SCON. The baud rate in this mode is 1/16 or 1/32 of the Timer 1 overflow, and since Timer 1 can be set to a wide range of values, a wide variation of baud rates is possible.

Transmission begins with a write to SBUF but is synchronized with the divide-by-16 counter, not the write to SBUF. The start bit is put on TxD at C1 following the first roll-over of the divide-by-16 counter, and the next bit is placed at C1 following the next rollover. After all eight bits are transmitted, the stop bit is transmitted. The TI flag is set in the next C1 state, or the tenth rollover of the divide-by-16 counter after the write to SBUF.

Reception is enabled when REN is high, and the serial port starts receiving data when it detects a falling edge on RxD. The falling-edge detector monitors the RxD line at 16 times the selected baud rate. When a falling edge is detected, the divide-by-16 counter is reset to align the bit boundaries with the rollovers of the counter. The 16 states of the counter divide the bit time into 16 slices. Bit detection is done on a best-of-three basis using samples at the 8th, 9th and 10th counter states. If the first bit after the falling edge is not 0, the start bit is invalid, reception is aborted immediately, and the serial port resumes looking for a falling edge on RxD. If a valid start bit is detected, the rest of the bits are shifted into SBUF. After shifting in eight data bits, the stop bit is received. Then, if

1. RI is 0 and
2. SM2 is 0 or the received stop bit is 1

the stop bit goes into RB8, the eight data bits go into SBUF, and RI is set. Otherwise, the received frame is lost. In the middle of the stop bit, the receiver resumes looking for a falling edge on RxD.

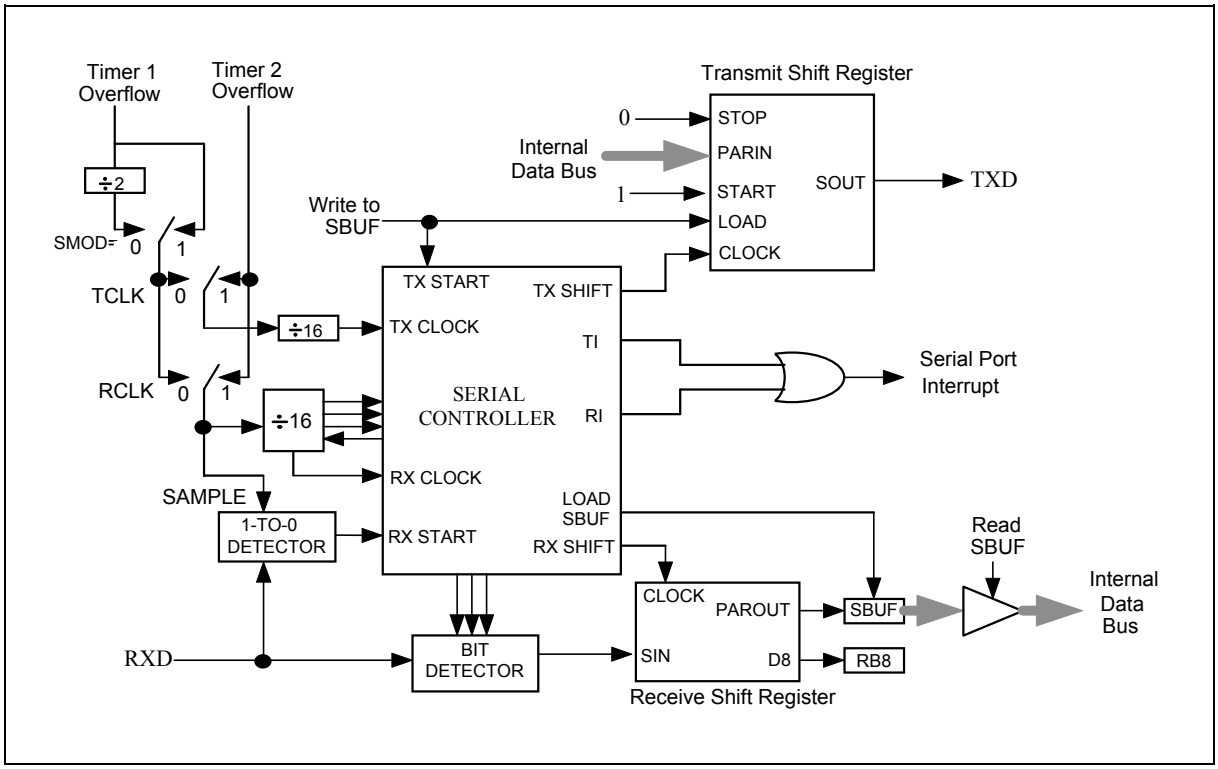


Figure 12-2 Serial Port Mode 1

12.3 Mode 2

In Mode 2, full-duplex asynchronous communication is used. Frames consist of eleven bits: one start bit (0), eight data bits (LSB first), a programmable ninth bit (TB8) and a stop bit (0). When receiving, the ninth bit is put into RB8. The baud rate is 1/16 or 1/32 of the oscillator frequency, as determined by SMOD in PCON.

Transmission begins with a write to SBUF but is synchronized with the divide-by-16 counter, not the write to SBUF. The start bit is put on TxD pin at C1 following the first roll-over of the divide-by-16 counter, and the next bit is placed on TxD at C1 following the next rollover. After all nine bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the next C1 state, or the 11th rollover of the divide-by-16 counter after the write to SBUF.

Reception is enabled when REN is high, and the serial port starts receiving data when it detects a falling edge on RxD. The falling-edge detector monitors the RxD line at 16 times the selected baud rate. When a falling edge is detected, the divide-by-16 counter is reset to align the bit boundaries with the rollovers of the counter. The 16 states of the counter divide the bit time into 16 slices. Bit detection is done on a best-of-three basis using samples at the 8th, 9th and 10th counter states. If the first bit after the falling edge is not 0, the start bit is invalid, reception is aborted, and the serial port resumes looking for a falling edge on RxD. If a valid start bit is detected, the rest of the bits are shifted into SBUF. After shifting in nine data bits, the stop bit is received. Then, if

1. RI is 0 and
2. SM2 is 0 or the received stop bit is 1

the stop bit goes into RB8, the eight data bits go into SBUF, and RI is set. Otherwise, the received frame may be lost. In the middle of the stop bit, the receiver resumes looking for a falling edge on RxD. The functional description is shown in the figure below.

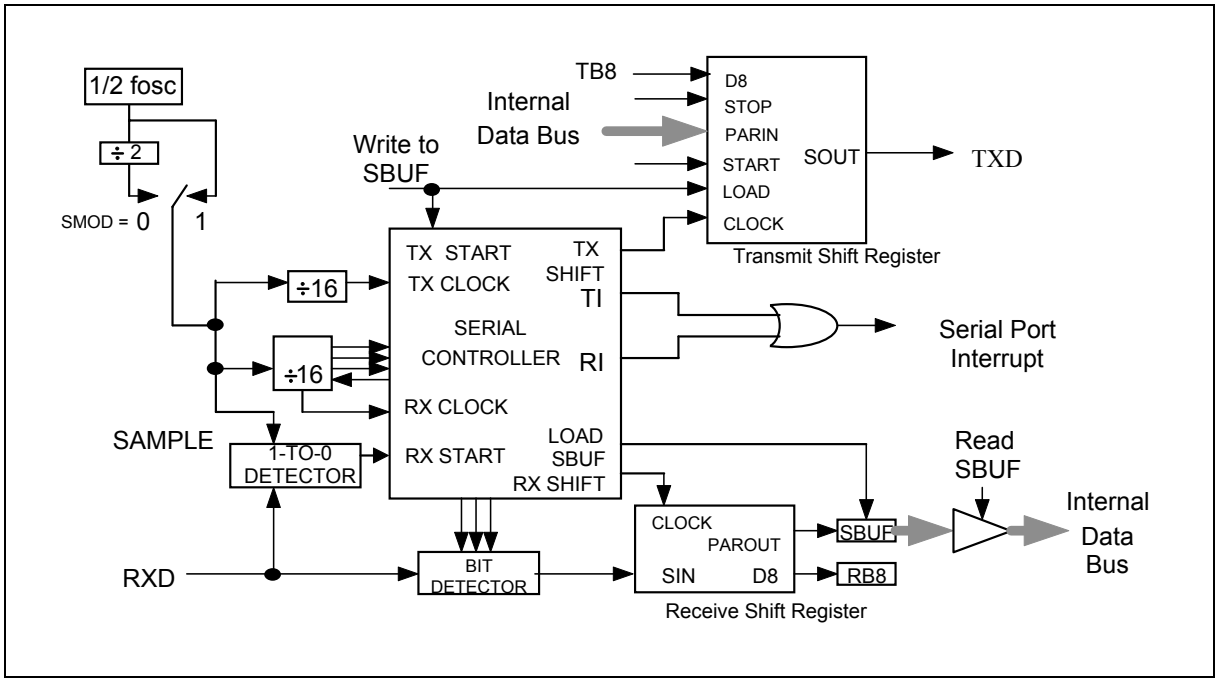


Figure 12-3 Serial Port Mode 2

12.4 Mode 3

This mode is the same as Mode 2, except that the baud rate is programmable. The program must select the mode and baud rate in SCON before any communication can take place. Timer 1 should be initialized if Mode 1 or Mode 3 will be used.

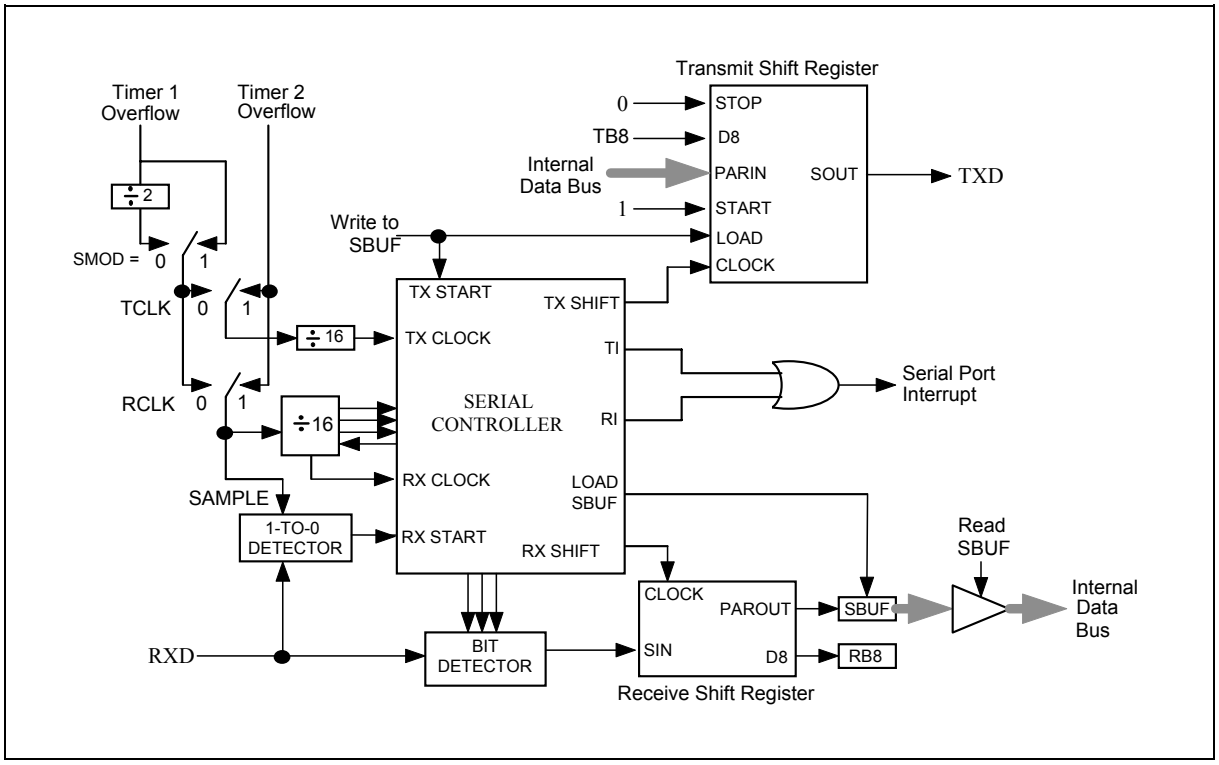


Figure 12-4 Serial Port Mode 3

Table 7 Serial Ports Modes

SM1	SM0	MODE	TYPE	BAUD CLOCK	FRAME SIZE	START BIT	STOP BIT	9TH BIT FUNCTION
0	0	0	Synch.	4 or 12 TCLKS	8 bits	No	No	None
0	1	1	Asynch.	Timer 1 or 2	10 bits	1	1	None
1	0	2	Asynch.	32 or 64 TCLKS	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1 or 2	11 bits	1	1	0, 1

12.5 Framing Error Detection

A frame error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically, a frame error is due to noise or contention on the serial communication line. The W79E201 has the ability to detect framing errors and set a flag that can be checked by software.

The frame error FE (FE_1) bit is located in SCON.7. This bit is SM0 in the standard 8051/52 family, but, in the W79E201, it serves a dual function and is called SM0/FE. There are actually two separate flags, SM0 and FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6). When SMOD0 is set to 1, the FE flag is accessed. When SMOD0 is set to 0, the SM0 flag is accessed.

The FE bit is set to 1 by the hardware, but it must be cleared by the software. Once FE is set, any frames received afterwards, even those without errors, do not clear the FE flag. The flag has to be cleared by the software. Note that SMOD0 must be set to 1 while reading or writing FE.

12.6 Multiprocessor Communications

Multiprocessor communication is available in modes 1, 2 and 3 and makes use of the 9th data bit and the automatic address recognition feature. This approach eliminates the software overhead required to check every received address and greatly simplifies the program.

In modes 2 and 3, address bytes are distinguished from data bytes by 9th bit set, which is set high in address bytes. When the master processor wants to transmit a block of data to one of the slaves, it first sends the address of the target slave(s). The slave processors have already set their SM2 bits high so that they are only interrupted by an address byte. The automatic address recognition feature then ensures that only the addressed slave is actually interrupted. This feature compares the received byte to the slave's Given or Broadcast address and only sets the RI flag if the bytes match. This slave then clears the SM2 bit, clearing the way to receive the data bytes. The unaddressed slaves are not affected, as they are still waiting for their address.

In mode 1, the 9th bit is the stop bit, which is 1 in valid frames. Therefore, if SM2 is 1, RI is only set if a valid frame is received and if the received byte matches the Given or Broadcast address.

The master processor can selectively communicate with groups of slaves using the Given Address or all the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN registers. The slave address is the 8-bit value specified in SADDR. SADEN is a mask for the value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is a don't-care condition in the address comparison. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This provides flexibility to address multiple slaves without changing addresses in SADDR.

The following example shows how to setup the Given Addresses to address different slaves.

Slave 1:

SADDR	1010 0100
SADEN	1111 1010
Given	1010 0x0x

Slave 2:

SADDR	1010 0111
SADEN	1111 1001
Given	1010 0xx1

The Given Address for slaves 1 and 2 differ in the LSB. In slave 1, it is a don't-care, while, in slave 2, it is 1. Thus, to communicate with only slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly, bit 1 is 0 for slave 1 and don't-care for slave 2. Hence, to communicate only with slave 2, the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. Since bit 3 is don't-care for both slaves, two different addresses can address both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously using the Broadcast Address. The Broadcast Address is formed from the logical OR of the SADDR and SADEN registers. The zeros in the result are don't–care values. In most cases, the Broadcast Address is FFh. In the previous case, the Broadcast Address is (1111111X) for slave 1 and (11111111) for slave 2.

The SADDR and SADEN registers are located at addresses A9h and B9h, respectively. These two registers default to 00h, so the Given Address and Broadcast Address default to XXXX XXXX (i.e., all bits don't-care), which effectively removes the multiprocessor communications feature

13. PULSE-WIDTH-MODULATED (PWM) OUTPUTS

There are six pulse-width-modulated (PWM) output channels that can generate pulses of programmable length and interval. The frequency is controlled by the 8-bit prescale PWMP, which supplies the clock for the 8-bit PWM counter that counts modular 255 (0 ~ 254). The same prescale and counter are shared by all the PWM channels. The PWM outputs are weakly pulled high.

Each channel is enabled and disabled by bit ENPWM*n* (n = 0 ~ 5). If channel *n* is enabled, the PWM counter is compared to the corresponding register PWM*n*. When PWM*n* is greater than the PWM counter, the corresponding PWM output is set high. When the register value is equal to or less than the counter value, the output is set low. Therefore, the pulse-width ratio is defined by the contents of PWM0, PWM1, PWM2, PWM3, PWM4 and PWM5 and may be programmed in increments of 1/255. This is illustrated below.

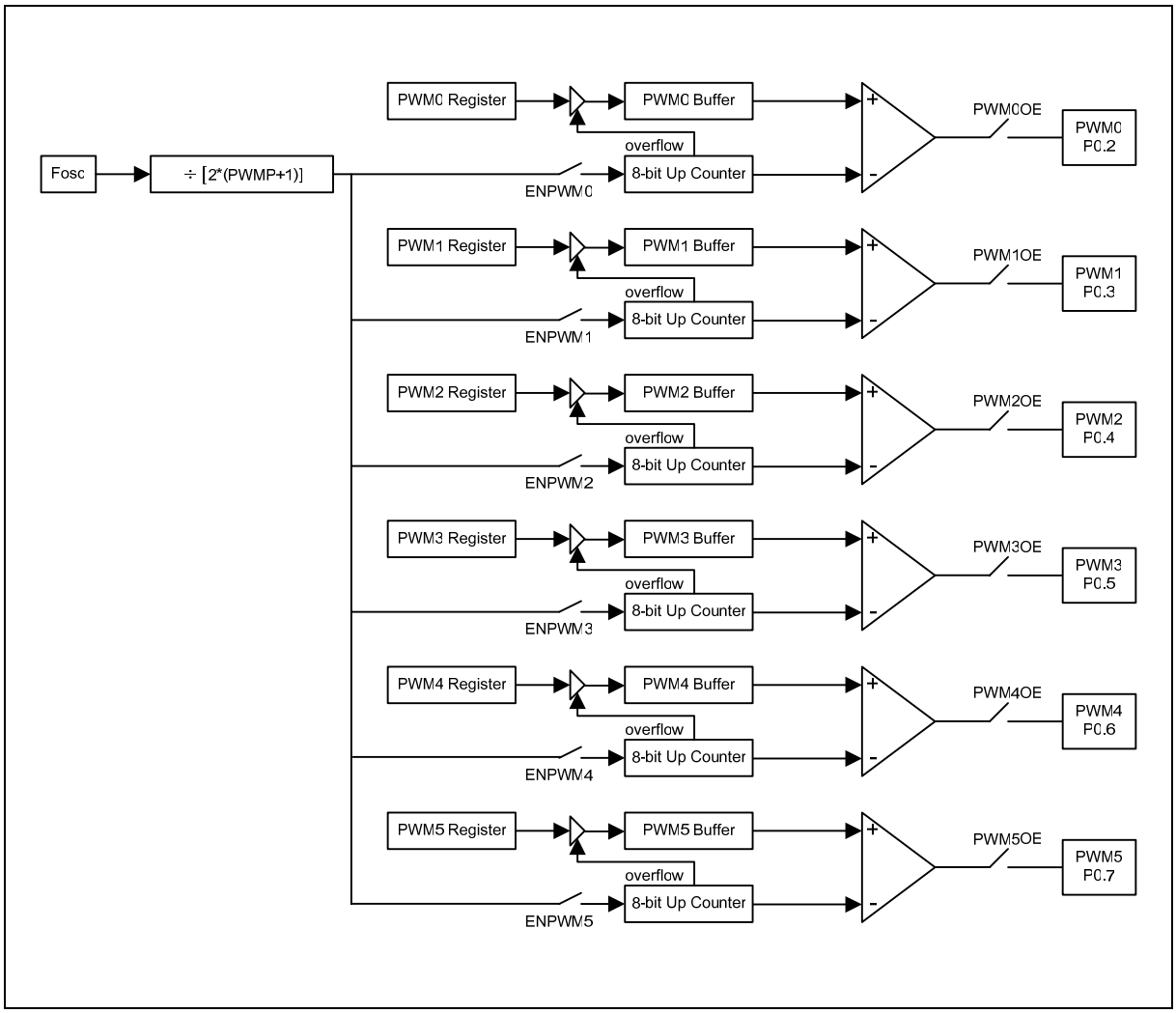


Figure 13-1 PWM block diagram

If register PWM*n* is loaded with a new value, the associated output is updated immediately. By loading PWM*n* with 00H or FFH, the corresponding channel provides a constant high or low level output, respectively.[1]

Buffered PWM outputs may be used to drive DC motors. In this case, the rotation speed of the motor is proportional to the contents of PWM*n*. The repetition frequency Fpwm for channel *n* is given by:

$$Fpwm = \frac{Fosc}{2 \times (1 + PWMP) \times 255}$$

Prescale division factor = PWM + 1

$$\text{PWMn high/low ratio of } PWMn = \frac{(PWMn)}{255 - (PWMn)}$$

This gives a repetition frequency range of 123 Hz to 31.4 KHz (f_{osc} = 16 MHz).

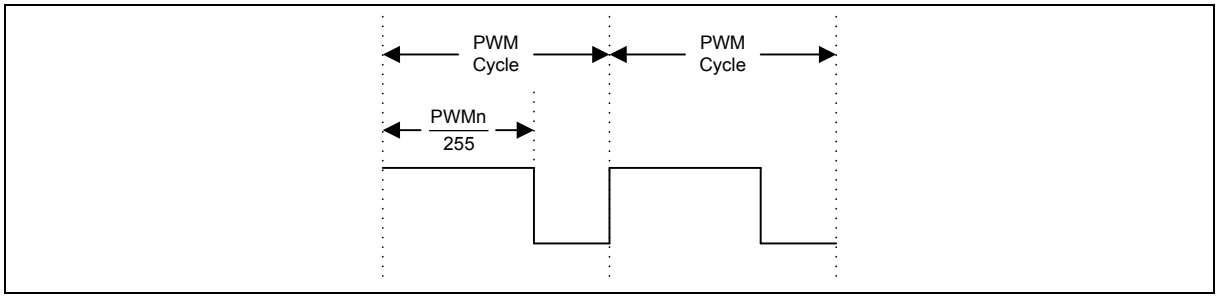


Figure 13-2 PWM Duty Cycle

[1] Since the 8-bit counter counts modulo 255, it can never actually reach FFh, so the output remains low all the time.

14. ANALOG-TO-DIGITAL CONVERTER (ADC)

The ADC converts one of eight analog input channels into a 10-bit value using successive approximation control logic. The conversion process takes 50 machine cycles to complete. The functional diagram is illustrated below.

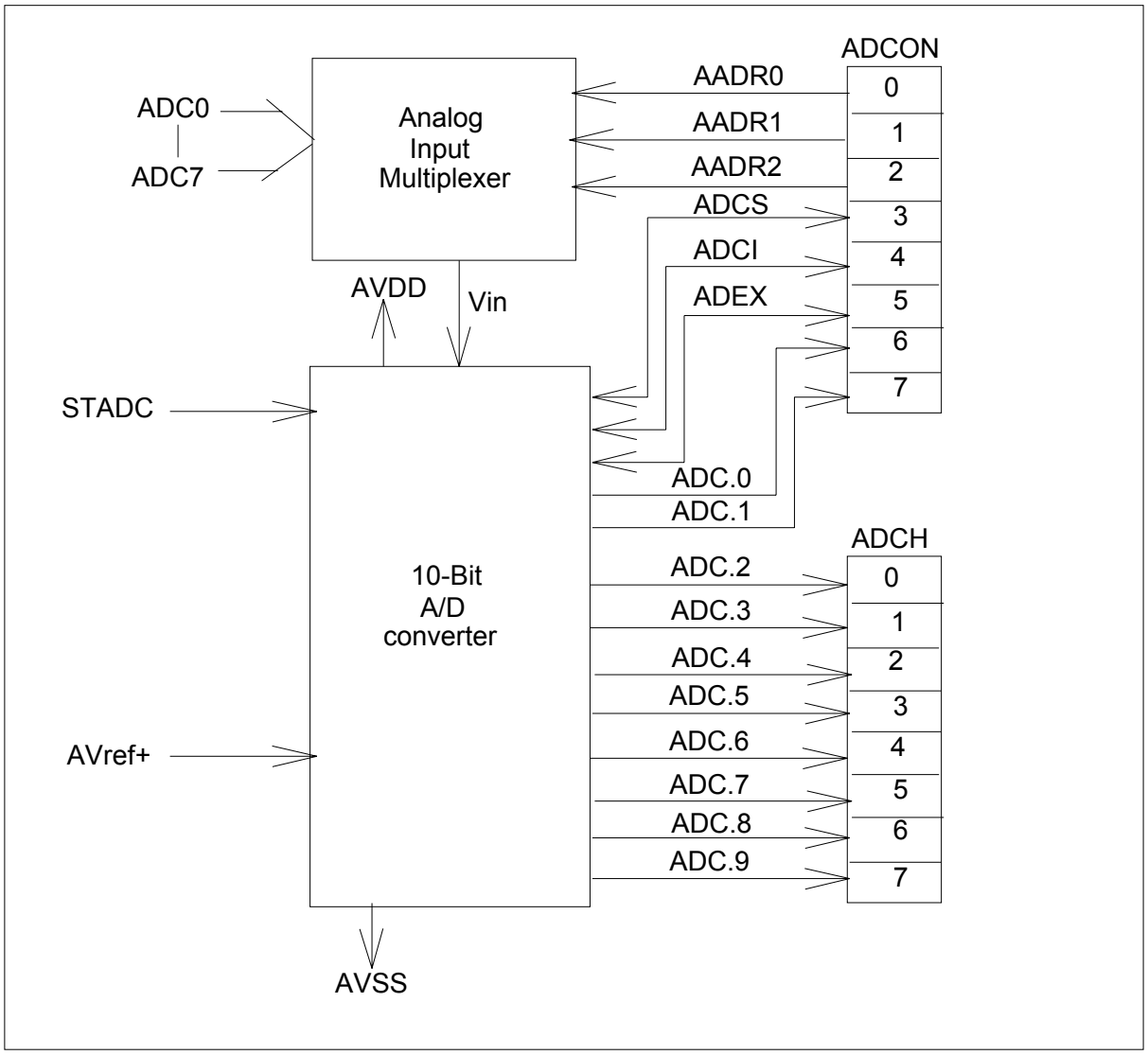


Figure 14-1 ADC Functional block Diagram

The ADC circuit is enabled by ADCCEN. Control bits ADCCON.0, ADCCON.1 and ADCCON.2 are connected to an analog multiplexer that selects one of eight analog channels to convert (Vin). A conversion is initiated by setting the ADCS bit (ADDCON.3). The ADCS bit can be set by either hardware (P2.0) or software, according to the ADEX bit (ADCCON.5). If ADEX is 0, only the software can set ADCS. If ADEX is 1, the software can set ADCS, or it can be set by applying a rising edge to external pin STADC. The rising edge must consist of a low level on STADC for at least one machine

cycle followed by a high level signal on STADC for at least one machine cycle, to make sure the W79E201 detects both parts of the transition. The low-to-high transition on STADC is then recognized at the end of a machine cycle, and the conversion commences at the beginning of the next cycle.

The ADC contains a digital-to-analog converter (DAC) that converts the contents of a successive approximation register to a voltage (V_{DAC}), which is compared to the analog input voltage (Vin). The output of the comparator is then fed back to the successive approximation control logic that controls the successive approximation register. This is illustrated in the figure below.

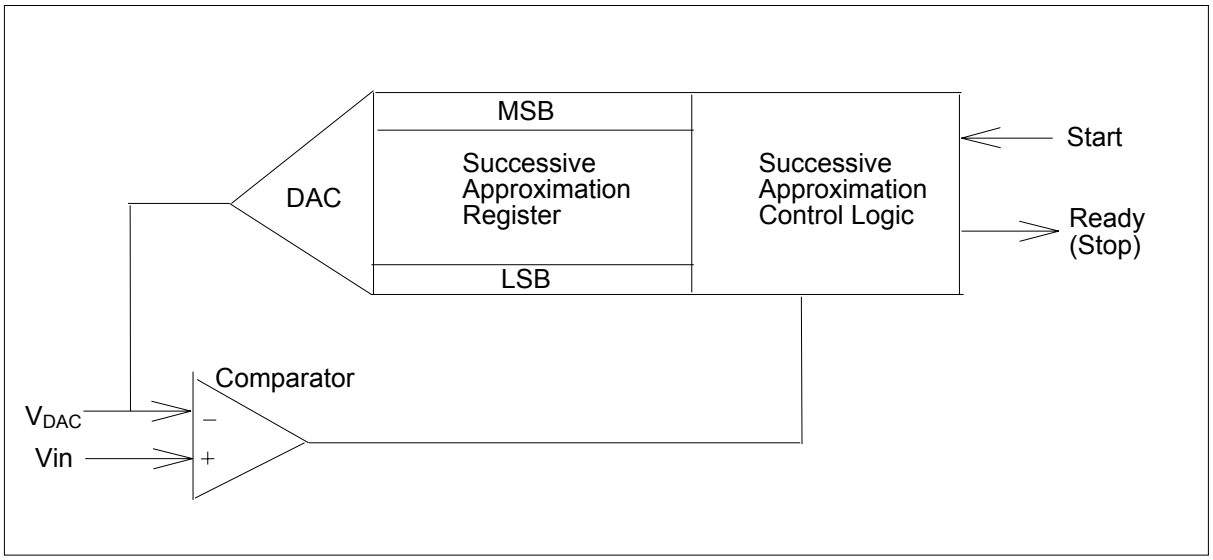


Figure 14-2 Successive Approximation ADC

The conversion takes 50 machine cycles, and the end of the conversion is flagged by ADCI (ADCCON.4). The result is a 10-bit value: the upper eight bits are stored in register ADCH, and the two LSB are stored in ADCCON, bits 7 and 6. The program may ignore the two LSB in ADCCON and use the 8-bit value in ADCH instead.

Once an ADC conversion is in progress, another ADC start (by the hardware or software) has no effect on it, but a conversion in progress is aborted if the W79E201 enters power-down mode. The result of a completed conversion (once ADCI is set to 1) is unaffected in this case, however.

The ADC has its own supply pins AVDD, AVSS and Vref+, which are connected to each end of the DAC's resistance-ladder. The ladder has 1023 equally-spaced taps, separated by a resistance R. The first tap is located 0.5 x R above AVss, and the last tap is located 0.5 x R below Vref+, giving a total ladder resistance of 1024 x R. This structure ensures that the DAC is monotonic and results in a symmetrical quantization error.

For input voltages between AVss and [(Vref+) + ½ LSB], the 10-bit result is 00 0000 0000b, or 000H. For input voltages between [(Vref+) – 3/2 LSB] and Vref+, the result is 11 1111 1111B, or 3FFH. AVref+ and AVss may be between (AV_{DD} + 0.2 V) and (AV_{SS} – 0.2 V), and Avref+ should be positive with respect to AVss. For input voltages between AVref+ and AVss, the result can be calculated from the formula: $\text{Result} = 1024 \times \frac{\text{Vin}}{AV_{ref+}}$

15. TIMED-ACCESS PROTECTION

The W79E201 has features like the Watchdog Timer, wait-state control signal and power-on/fail reset flag that are crucial to the proper operation of the system. If these features are unprotected, errant code may write critical control bits, resulting in incorrect operation and loss of control. To prevent this, the W79E201 provides has a timed-access protection scheme that controls write access to critical bits.

In this scheme, protected bits have a timed write-enable window. A write is successful only if this window is active; otherwise, the write is discarded. The write-enable window is opened in two steps. First, the software writes AAh to the Timed Access (TA) register. This starts a counter, which expires in three machine cycles. Then, if the software writes 55h to the TA register before the counter expires, the write-enable window is opened for three machine cycles. After three machine cycles, the window automatically closes, and the procedure must be repeated again to access protected bits.

The suggested code for opening the write-enable window is

```
TA    REG   0C7h          ; Define new register TA, located at 0C7h
      MOV   TA, #0AAh
      MOV   TA, #055h
```

Five examples, some correct and some incorrect, of using timed-access protection are shown below.

Example 1: Valid access

```
      MOV   TA, #0AAh          3 M/C   ; Note: M/C = Machine Cycles
      MOV   TA, #055h          3 M/C
      MOV   WDCON, #00h        3 M/C
```

Example 2: Valid access

```
      MOV   TA, #0AAh          3 M/C
      MOV   TA, #055h          3 M/C
      NOP                      1 M/C
      SETB  EWT                2 M/C
```

Example 3: Valid access

```
      MOV   TA, #0Aah          3 M/C
      MOV   TA, #055h          3 M/C
      ORL   WDCON, #00000010B  3M/C
```

Example 4: Invalid access

```
      MOV   TA, #0AAh          3 M/C
      MOV   TA, #055h          3 M/C
      NOP                      1 M/C
      NOP                      1 M/C
      CLR   POR                2 M/C
```

Example 5: Invalid Access

```
MOV   TA, #0AAh      3 M/C
NOP                  1 M/C
MOV   TA, #055h      3 M/C
SETB  EWT            2 M/C
```

In the first three examples, the protected bits are written before the window closes. In Example 4, however, the write occurs after the window has closed, so there is no change in the protected bit. In Example 5, the second write to TA occurs four machine cycles after the first write, so the timed access window in not opened at all, and the write to the protected bit fails.

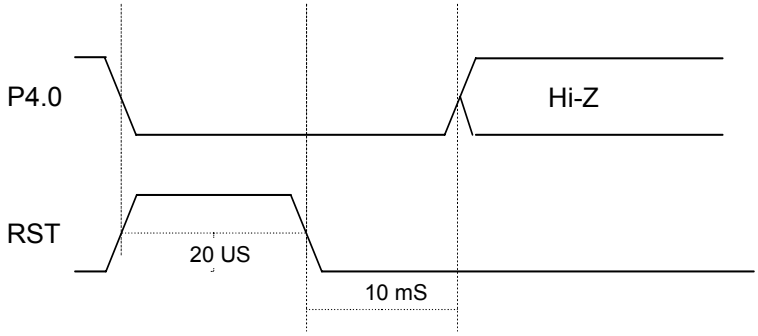
16. H/W REBOOT MODE (BOOT FROM 4K BYTES OF LD FLASH EPROM)

The W79E201 boots from the AP Flash EPROM (16 KB) by default during an external reset. It is possible to boot from the LD Flash EPROM program (4 KB) instead. This is explained below. Note that it is necessary to add a 10-KΩ resistor on pin P4.0 to do this.

Reboot Mode

OPTION BITS	RST	P4.0	MODE
Bit3 L	H	L	REBOOT

The Reset Timing For Entering REBOOT Mode



Notes:

1: In application system design, user must take care the P4.0, ALE, /EA and /PSEN pin value at reset to avoid W79E201 entering the programming mode or REBOOT mode in normal operation.

17. IN-SYSTEM PROGRAMMING

This section explains the key steps to use in-system programming. The steps depend on whether the loader program is located in the LD Flash EPROM or AP Flash EPROM, although both processes begin while the W79E201 is running with the AP Flash EPROM.

If the loader program is located in the LD Flash EPROM, the main program should set CHPCON to 03H, and then enter idle mode. When the W79E201 wakes up, the CPU switches to the LD Flash EPROM and executes a reset. (This reset switches to LD Flash EPROM memory too.) The loader program then sets the SFRCN register to update the AP Flash EPROM, and, afterwards, it requests a software reset (CHPCON = 83H) to switch back to the AP Flash EPROM. The CPU restarts using the updated program in the AP Flash EPROM.

If the loader program is located in the AP Flash EPROM, the main program should set CHPCON to 01H, and then enter idle mode. The loader program then sets the SFRCN register to update the LD Flash EPROM, and, afterwards, the CPU continues to run the program in the AP Flash EPROM.

Please see the In-system Programming Software Examples for additional details and code examples.

18. SECURITY BITS

The security bits protect the code and data inside the Flash EPROM and Special Setting Registers from various risks. These bits are enabled by setting them low, and, once enabled, they cannot be changed, except by erasing the whole chip. The bit definitions are shown below.

Reserved	B3	B2	B1	B0	**Security Bits**

B3: 0 -> Enable H/W reboot with P4.0
B2: 0 -> Encryption
B1: 0 -> MOVC Inhibuted
B0: 0 -> Data out lock
Default 1 for each bit.

Each bit is explained separately.

B0: Lock bit

This bit is used to protect the code in the W79E201. Once this bit is set to 0, Flash EPROM data (in both Flash EPROM) and the Special Setting Registers cannot be accessed again.

B1: MOVC Inhibit

This bit can prevent MOVC instructions in external memory from reading internal program code. When this bit is set to 0, MOVC instructions in external memory can only access code in external memory, not in internal memory. MOVC instructions in internal memory can always access both internal and external memory. If this bit is set to 1, there are no restrictions on the MOVC instruction.

B2: Encryption

This bit enables and disables the encryption logic for code protection. Once encryption is enabled, data presented on Port 0 is encoded.

B3: H/W Reboot with P4.0

If this bit is set to 0, the W79E201 can reboot from the LD Flash EPROM if RST =H and P4.0 = L. The program in the LD Flash EPROM may update the program in the AP Flash EPROM.

19. THE PERFORMANCE CHARACTERISTIC OF ADC

The offset error is the deviation between the ideal transfer value and actual transfer value. The gain error is the difference between the slope of the ideal transfer curve and the slope of actual transfer curve. The differential non-linearity (DNL) is the difference between the actual step width and ideal step width. The ideal step width is 1 LSB. The characteristics of DNL are shown in Figure 19-1 below.

$V_{DD} - V_{SS}$ = 5V ±10%, $AV_{DD} - V_{SS}$ =5V, Vref=5V, T_A = 25°C, Fosc = 16 MHz

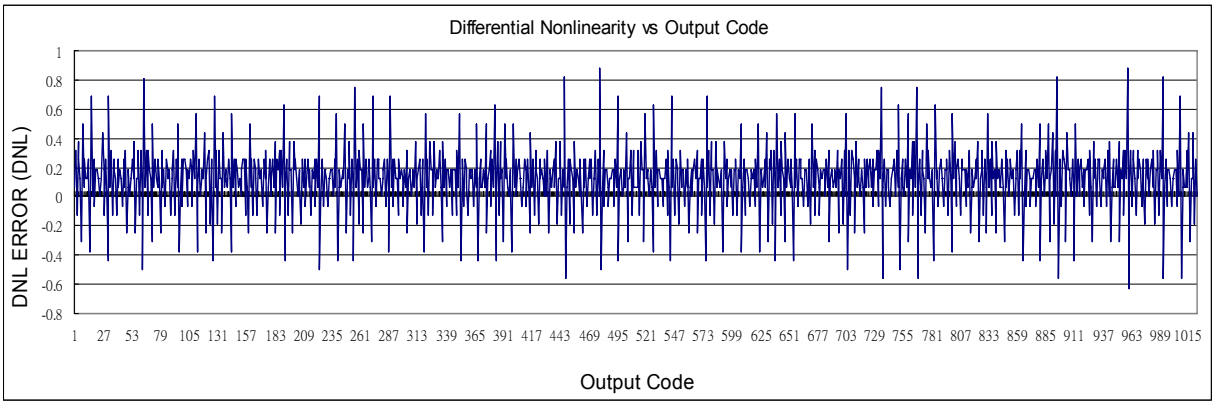


Figure 19-1 Differential Nonlinearity vs. Output Code

The integral non-linearity (INL) is the deviation of a code from the actual straight line. The deviation of each code is measured from the middle of the code. The characteristics of INL are shown in Figure 19-2 below.

$V_{DD} - V_{SS}$ = 5V ±10%, $AV_{DD} - V_{SS}$ = 5V, Vref = 5V, T_A = 25°C, Fosc = 16 MHz

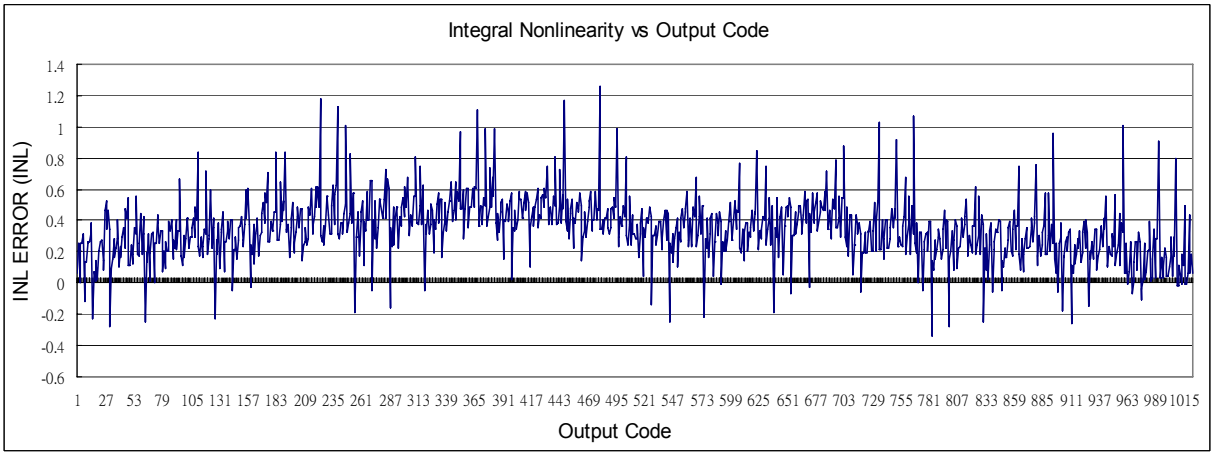


Figure 19-2 Integral Nonlinearity vs. Output Code

20. ELECTRICAL CHARACTERISTICS

20.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITION	RATING	UNIT
DC Power Supply	$V_{DD} - V_{SS}$	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	+70	°C
Storage Temperature	Tst	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

20.2 DC Characteristics

($V_{DD} - V_{SS}$ = 5V ±10%, T_A = 25°C, Fosc = 16 MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Operating Voltage	V_{DD}	4.5	5.5	V	
Operating Current	I_{DD}	-	30	mA	No load V_{DD} = RST = 5.5V
Idle Current	I_{IDLE}	-	24	mA	Idle mode V_{DD} = 5.5V
Power Down Current	I_{PWDN}	-	10	µA	Power-down mode V_{DD} = 5.5V
Input Current P1, P2, P3	I_{IN1}	-70	+10	µA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
Input Current RST[*1]	I_{IN2}	-10	+120	µA	V_{DD} = 5.5V 0<V_{IN}<V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	µA	V_{DD} = 5.5V 0V<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3	I_{TL}[*4]	-750	-200	µA	V_{DD} = 5.5V V_{IN} = 2.0V
Input Low Voltage P0, P1, P2, P3, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage RST[*1]	V_{IL2}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage XTAL1[*3]	VIL3	0	0.8	V	VDD = 4.5V

DC Characteristics, continued

PARAMETER	SYMBOL	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Input High Voltage P0, P1, P2, P3, $\overline{EA}$	V_{IH1}	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage RST	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage XTAL1[*3]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Sink current P1, P3	I_{SK1}	4	15	mA	V_{DD} =4.5V Vs = 0.45V
Sink current P0,P2, ALE, $\overline{PSEN}$	I_{SK2}	8	15	mA	V_{DD} =4.5V V_{OL} = 0.45V
Source current P1, P3	I_{SR1}	-180	-360	uA	V_{DD} =4.5V V_{OL} = 2.4V
Source current P0, P2, ALE, $\overline{PSEN}$	I_{SR2}	-10	-14	mA	V_{DD} =4.5V V_{OL} = 2.4V
Output Low Voltage P1, P3	V_{OL1}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +6 mA
Output Low Voltage P0, P2, ALE, $\overline{PSEN}$ [*2]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +10 mA
Output High Voltage P1, P3	V_{OH1}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -180 μA
Output High Voltage P0, P2, ALE, $\overline{PSEN}$ [*2]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -10mA

Notes:

*1. RST pin is a Schmitt trigger input.

*2. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

*3. XTAL1 is a CMOS input.

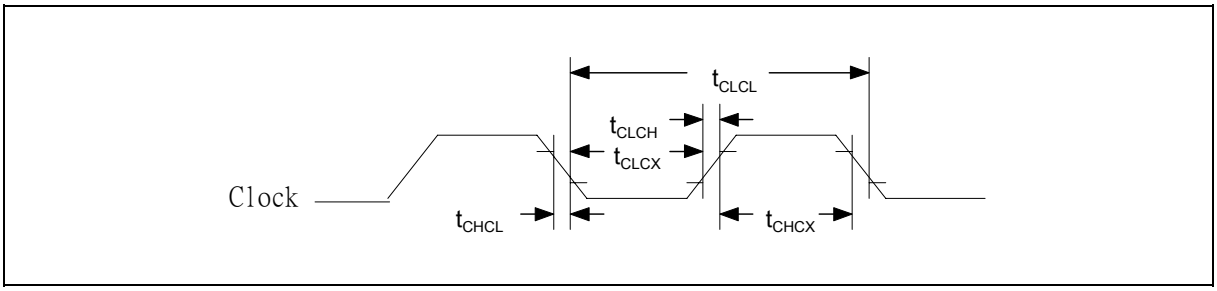
*4. Pins of P1, P2 and P3 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when VIN approximates to 2V.

20.3 ADC DC Electrical Characteristics

(AV_{DD} - AV_{SS}= 5V±10%, T_A= 25°C, Fosc = 16MHz, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Analog input	AVin	AVSS-0.2	AVDD+0.2	V	
Reference voltage	AVref	-	AVDD+0.2	V	
Resistance between AVref and AVSS	Rref	10	50	KΩ	When ADC is enabled
Conversion time	t_C		$52t_{MC}$	μs	t_{MC} is machine cycle
Offset error	Ofe	-2	+2	LSB	
Gain error	Ge	-0.4	+0.4	%	
Differential non-linearity	DNL	-1	+1	LSB	
Integral non-linearity	INL	-2	+2	LSB	

20.4 AC Characteristics



Note: Duty cycle is 50%.

External Clock Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t_{CHCX}	12	-	-	ns	
Clock Low Time	t_{CLCX}	12	-	-	ns	
Clock Rise Time	t_{CLCH}	-	-	10	ns	
Clock Fall Time	t_{CHCL}	-	-	10	ns	

20.4.1 AC Specification

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Oscillator Frequency	$1/t_{CLCL}$	0	16	MHz
ALE Pulse Width	t_{LHLL}	$1.5t_{CLCL}$ - 5		ns
Address Valid to ALE Low	t_{AVLL}	$0.5t_{CLCL}$ - 5		ns
Address Hold After ALE Low	t_{LLAX1}	$0.5t_{CLCL}$ - 5		ns
Address Hold After ALE Low for MOVX Write	t_{LLAX2}	$0.5t_{CLCL}$ - 5		ns
ALE Low to Valid Instruction In	t_{LLIV}		$2.5t_{CLCL}$ - 20	ns
ALE Low to PSEN Low	t_{LLPL}	$0.5t_{CLCL}$ - 5		ns
$\overline{\text{PSEN}}$ Pulse Width	t_{PLPH}	$2.0t_{CLCL}$ - 5		ns
$\overline{\text{PSEN}}$ Low to Valid Instruction In	t_{PLIV}		$2.0t_{CLCL}$ - 20	ns
Input Instruction Hold After PSEN	t_{PXIX}	0		ns
Input Instruction Float After PSEN	t_{PXIZ}		t_{CLCL} - 5	ns
Port 0 Address to Valid Instr. In	t_{AVIV1}		$3.0t_{CLCL}$ - 20	ns
Port 2 Address to Valid Instr. In	t_{AVIV2}		$3.5t_{CLCL}$ - 20	ns
$\overline{\text{PSEN}}$ Low to Address Float	t_{PLAZ}	0		ns
Data Hold After Read	t_{RHDX}	0		ns
Data Float After Read	t_{RHDZ}		t_{CLCL} - 5	ns
$\overline{\text{RD}}$ Low to Address Float	t_{RLAZ}		$0.5t_{CLCL}$ - 5	ns

20.4.2 MOVX Characteristics Using Stretch Memory Cycle

PARAMETER	SYM.	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS	STRECH
Data Access ALE Pulse Width	t_{LLHL2}	$1.5t_{CLCL}$ - 5 $2.0t_{CLCL}$ - 5		ns	t_{MCS} = 0 t_{MCS}>0
Address Hold After ALE Low for MOVX write	t_{LLAX2}	$0.5t_{CLCL}$ - 5		ns	
$\overline{RD}$ Pulse Width	t_{RLRH}	$2.0t_{CLCL}$ - 5 t_{MCS} - 10		ns	t_{MCS} = 0 t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2.0t_{CLCL}$ - 5 t_{MCS} - 10		ns	t_{MCS} = 0 t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2.0t_{CLCL}$ - 20 t_{MCS} - 20	ns	t_{MCS} = 0 t_{MCS}>0
Data Hold after Read	t_{RHDX}	0		ns	
Data Float after Read	t_{RHDZ}		t_{CLCL} - 5 $2.0t_{CLCL}$ - 5	ns	t_{MCS} = 0 t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$ - 5 t_{MCS} + $2t_{CLCL}$ - 40	ns	t_{MCS} = 0 t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3.0t_{CLCL}$ - 20 $2.0t_{CLCL}$ - 5	ns	t_{MCS} = 0 t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$ - 5 $1.5t_{CLCL}$ - 5	$0.5t_{CLCL}$ + 5 $1.5t_{CLCL}$ + 5	ns	t_{MCS} = 0 t_{MCS}>0
Port 0 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL}	t_{CLCL} - 5 $2.0t_{CLCL}$ - 5		ns	t_{MCS} = 0 t_{MCS}>0
Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL}$ - 5 $2.5t_{CLCL}$ - 5		ns	t_{MCS} = 0 t_{MCS}>0
Data Valid to WR Transition	t_{QVWX}	-5 $1.0t_{CLCL}$ - 5		ns	t_{MCS} = 0 t_{MCS}>0
Data Hold after Write	t_{WHQX}	t_{CLCL} - 5 $2.0t_{CLCL}$ - 5		ns	t_{MCS} = 0 t_{MCS}>0
$\overline{RD}$ Low to Address Float	t_{RLAZ}		$0.5t_{CLCL}$ - 5	ns	
$\overline{RD}$ or WR high to ALE high	t_{WHLH}	0 $1.0t_{CLCL}$ - 5	10 $1.0t_{CLCL}$ + 5	ns	t_{MCS} = 0 t_{MCS}>0

Note: The t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the time period of the t_{MCS} for each selection of the Stretch value.

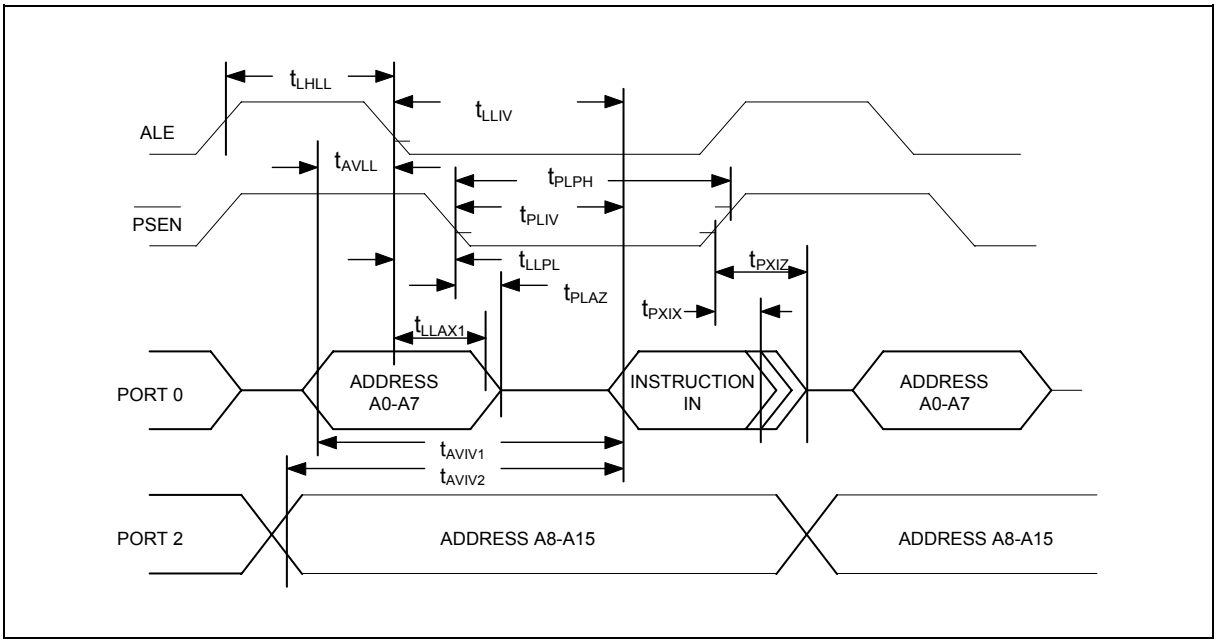
M2	M1	M0	MOVX CYCLES	T_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

Explanation of Logics Symbols

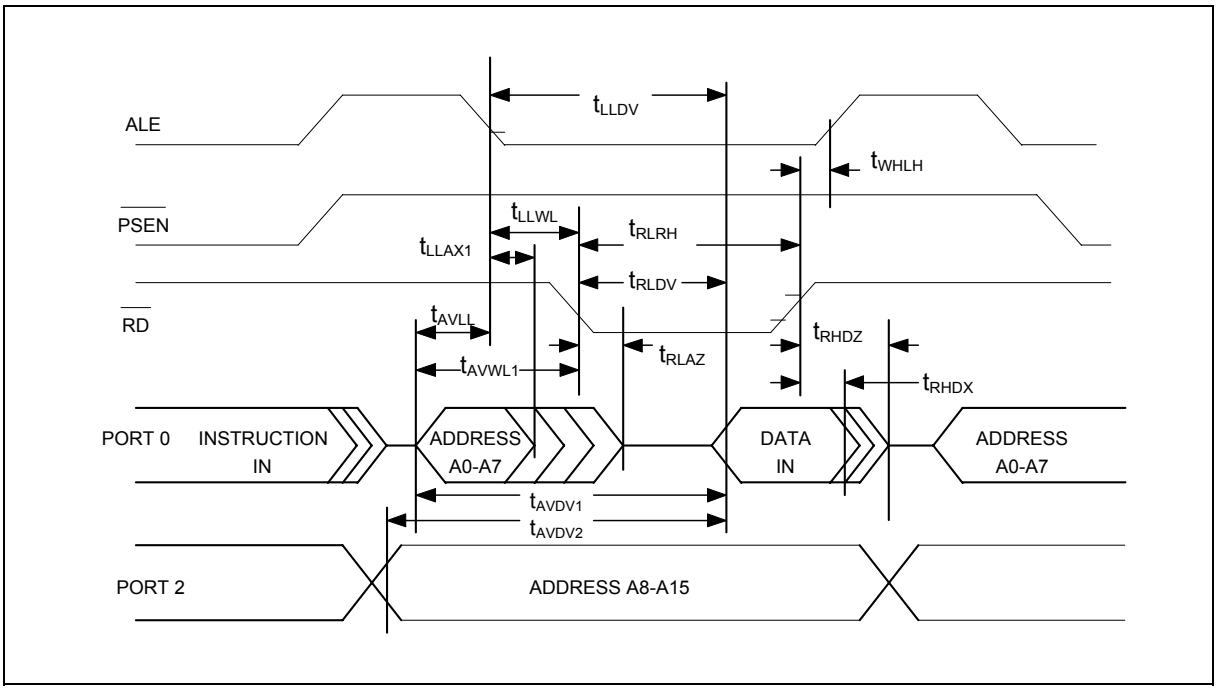
In order to maintain compatibility with the original 8051/52 family, this device specifies the same parameter for each device, using the same symbols. The explanation of the symbols is as follows.

t	Time	A	Address
C	Clock	D	Input Data
H	Logic level high	L	Logic level low
I	Instruction	P	$\overline{PSEN}$
Q	Output Data	R	$\overline{RD}$ signal
V	Valid	W	$\overline{WR}$ signal
X	No longer a valid state	Z	Tri-state

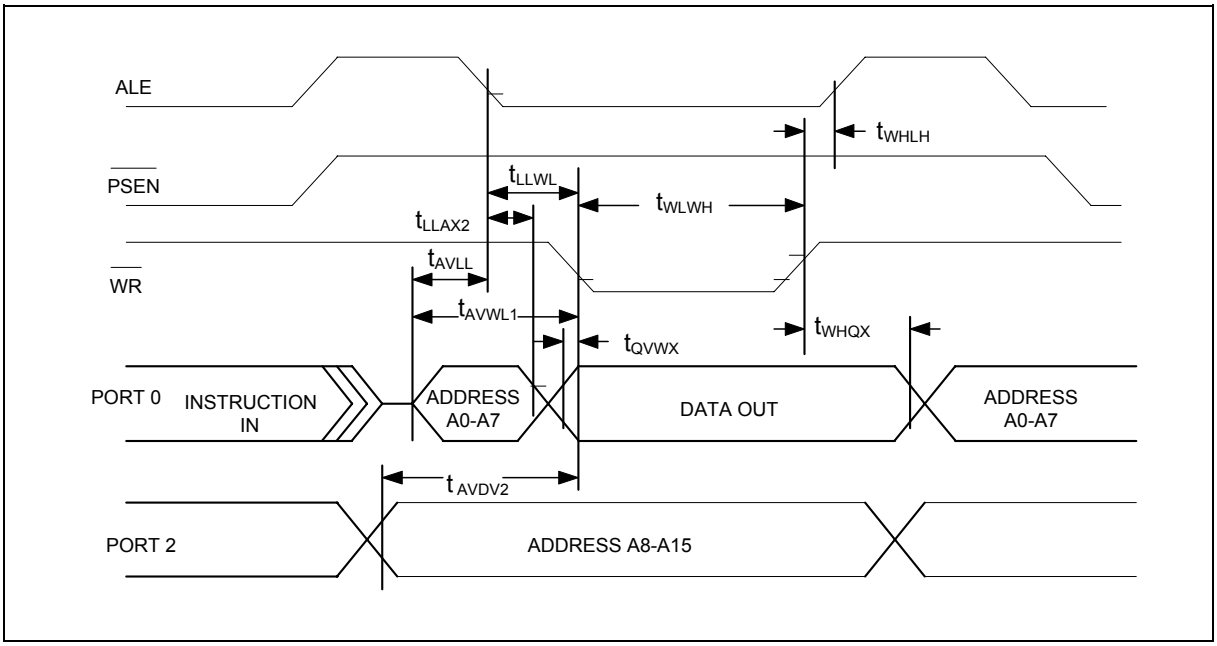
20.4.3 Program Memory Read Cycle



20.4.4 Data Memory Read Cycle



20.4.5 Data Memory Write Cycle



21. TYPICAL APPLICATION CIRCUITS

Expanded External Program Memory and Crystal

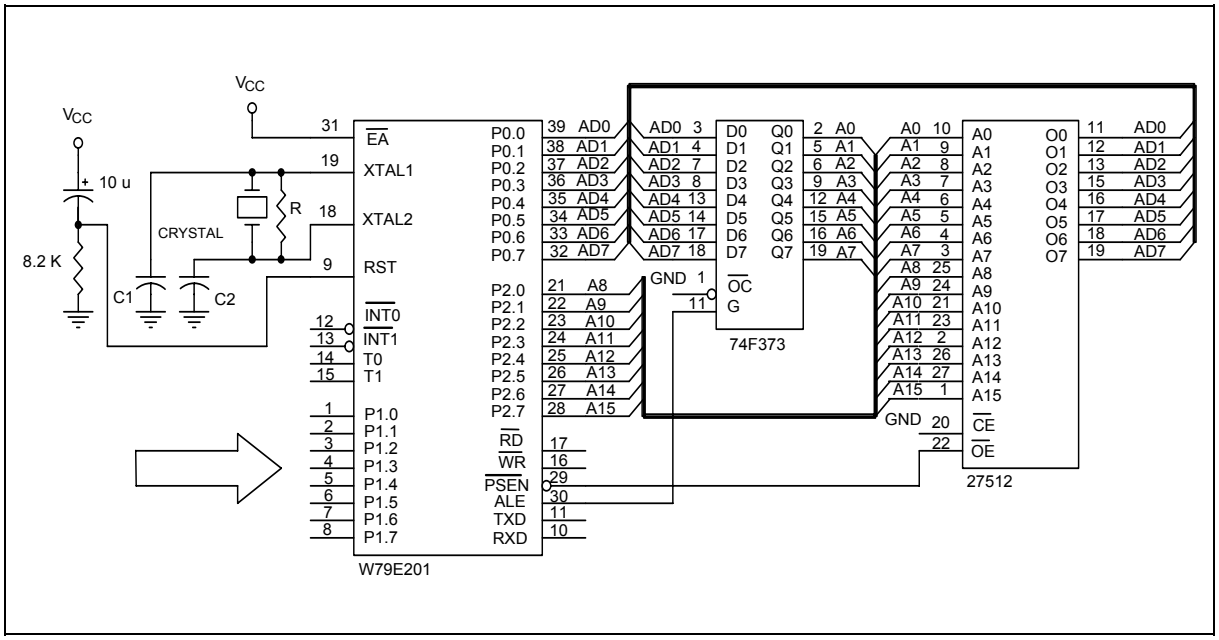


Figure A

CRYSTAL	C1	C2	R
12 MHz	Not necessary	Not necessary	Not necessary
16 MHz	Not necessary	Not necessary	Not necessary

Pull $\overline{EA}$ high to let the CPU fetch code in the embedded flash ROM, as long as the program counter is lower than 16K. When the program counter is higher than 16K, the CPU automatically fetches program code from extended external program memory.

Expanded External Data Memory and Oscillator

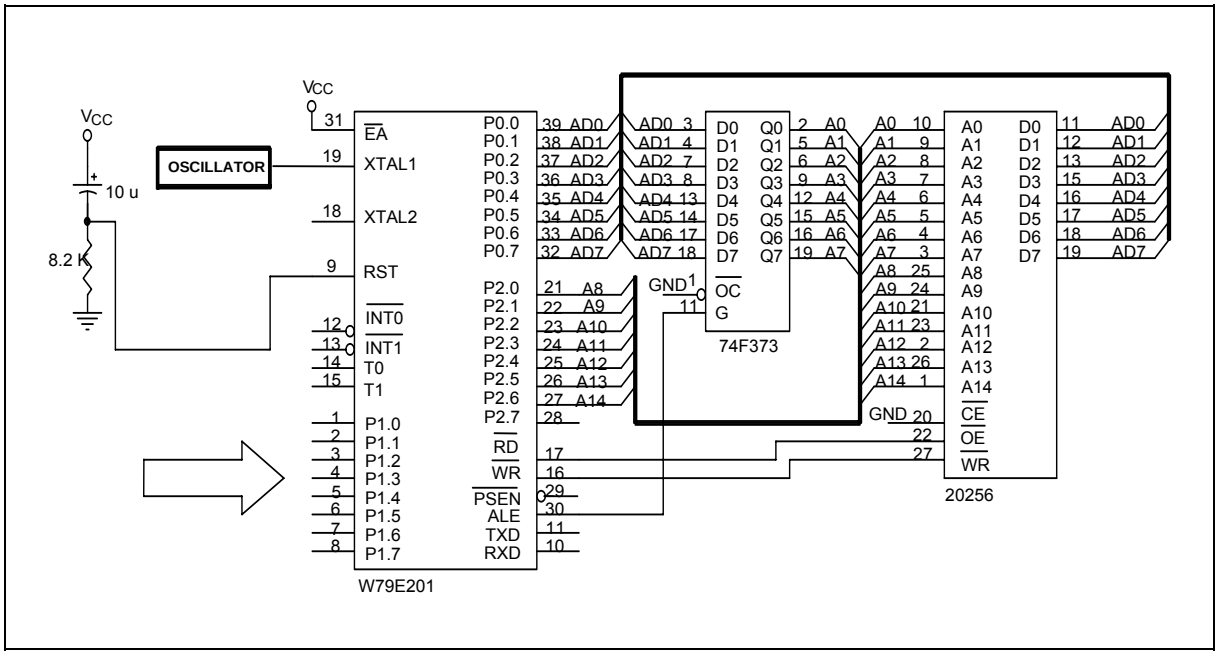
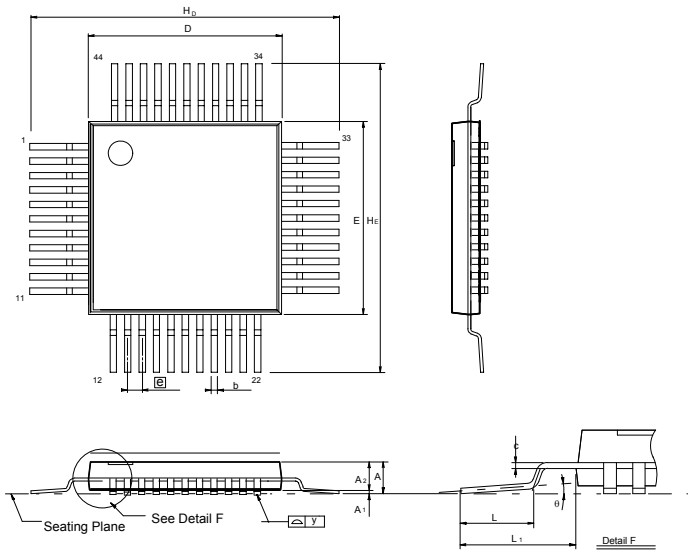


Figure B

22. PACKAGE DIMENSIONS

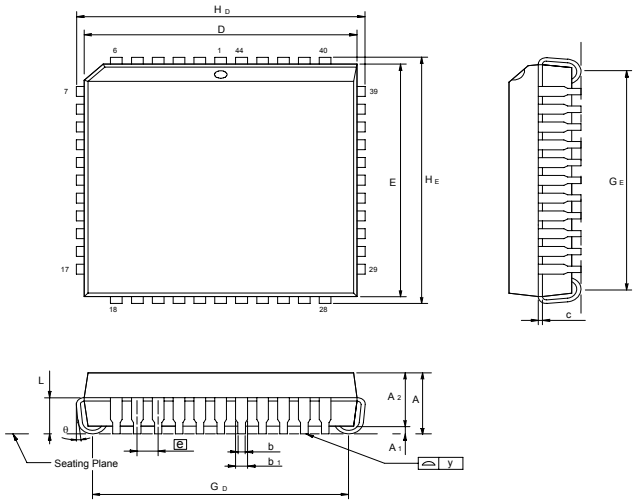
44-pin QFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

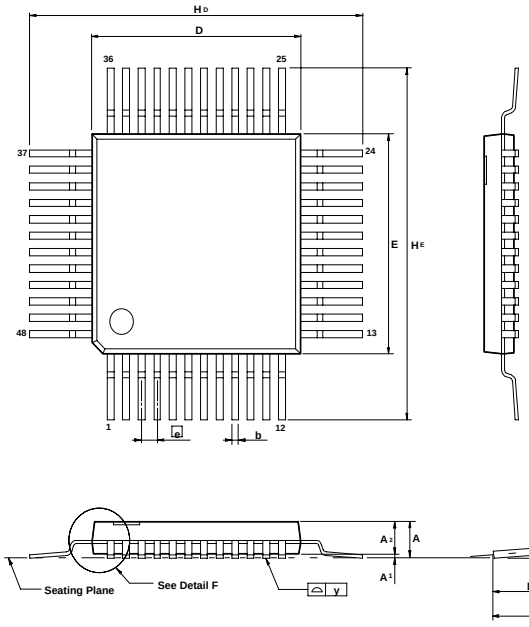
44-pin PLCC



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

48-pin LQFP



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	---	---	1.60
A_1	0.05	---	0.15
A_2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	---	0.20
D		7.00	
E		7.00	
e		0.50	
H_D		9.00	
H_E		9.00	
L	0.45	0.60	0.75
L_1		1.00	
y	---	0.08	---
θ	0	3.5°	7

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

23. IN-SYSTEM PROGRAMMING SOFTWARE EXAMPLES

This application note illustrates the in-system programmability of the Winbond W79E201 Flash EPROM microcontroller. In this example, microcontroller boots from the AP Flash EPROM and waits for a key to enter ISP mode to re-program the AP Flash EPROM. While in ISP mode, the microcontroller executes the loader program in the LD Flash EPROM. The loader program erases the AP Flash EPROM and then loads the new code from an external SRAM buffer.

If an application uses the reboot mode to update the program, the writer should enable security bit 3. See Security Bits for more information.

EXAMPLE 1:

```
;*********************************************************************************************************
;* Example of 16KB AP Flash EPROM program: Program will scan the P1.0. if P1.0 = 0, enters in-system
;* programming mode for updating the content of AP Flash EPROM code else executes the current ROM code.
;* XTAL = 16 MHz
;*********************************************************************************************************
                .chip 8052
                .RAMCHK OFF
                .symbols

CHPCON          EQU             9FH
TA              EQU             C7H
SFRAL           EQU             ACH
SFRAH           EQU             ADH
SFRFD           EQU             AEH
SFRCN           EQU             AFH

                ORG     0H
        LJMP    100H            ; JUMP TO MAIN PROGRAM
  ;*********************************************************************
  ;*  TIMER0 SERVICE VECTOR ORG = 000BH
  ;*********************************************************************
                ORG     00BH
        CLR     TR0             ; TR0 = 0, STOP TIMER0
        MOV     TL0,R6
        MOV     TH0,R7
        RETI

;*********************************************************************
;*  16K AP Flash EPROM MAIN PROGRAM
;*********************************************************************
                ORG     100H
```

```
MAIN_16K:
        MOV     A,P1            ; SCAN P1.0
        ANL     A,#01H
        CJNE    A,#01H,PROGRAM_16K   ; IF P1.0 = 0, ENTER IN-SYSTEM PROGRAMMING MODE
        JMP     NORMAL_MODE
PROGRAM_16:
        MOV     TA, #AAH        ; CHPCON register is written protect by TA register.
        MOV     TA, #55H
        MOV     CHPCON, #03H  ; CHPCON = 03H, ENTER IN-SYSTEM PROGRAMMING MODE
        MOV     SFRCN, #0H
        MOV     TCON, #00H      ; TR = 0 TIMER0 STOP
        MOV     IP, #00H        ; IP = 00H
        MOV     IE, #82H        ; TIMER0 INTERRUPT ENABLE FOR WAKE-UP FROM IDLE MODE
        MOV     R6, #F0H        ; TL0 = F0H
        MOV     R7, #FFH        ; TH0 = FFH
        MOV     TL0, R6
        MOV     TH0, R7
        MOV     TMOD, #01H      ; TMOD = 01H, SET TIMER0 A 16-BIT TIMER
        MOV     TCON, #10H      ; TCON = 10H, TR0 = 1,GO
        MOV     PCON, #01H      ; ENTER IDLE MODE FOR LAUNCHING THE IN-SYSTEM

PROGRAMMING
;************** ********************************************************************
;* Normal mode 16KB AP Flash EPROM program: depending user's application
;*******************************************************************************
NORMAL_MODE:
                .
        ; User's application program
                .
                .
                .
```

EXAMPLE 2:

```
;*****************************************************************************************************************
;* Example of 4KB LD Flash EPROM program: This loader program will erase the 16KB AP Flash EPROM first,
;* then reads the new code from external SRAM and program them into 16KB AP Flash EPROM.
;* XTAL = 16 MHz
;*****************************************************************************************************************
                .chip 8052
                .RAMCHK OFF
                .symbols

CHPCON          EQU             9FH
TA              EQU             C7H
SFRAL           EQU             ACH
SFRAH           EQU             ADH
SFRFD           EQU             AEH
SFRCN           EQU             AFH

                ORG     000H
        LJMP    100H            ; JUMP TO MAIN PROGRAM
;*********************************************************************
;* 1. TIMER0 SERVICE VECTOR ORG = 0BH
;*********************************************************************
                ORG     000BH
        CLR     TR0             ; TR0 = 0, STOP TIMER0
        MOV     TL0, R6
        MOV     TH0, R7
        RETI
;*********************************************************************
;*  4KB LD Flash EPROM MAIN PROGRAM
;*********************************************************************
                ORG     100H
MAIN_4K:
        MOV     TA,#AAH
        MOV     TA,#55H
        MOV     CHPCON,#03H   ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV     SFRCN,#0H
        MOV     TCON,#00H     ; TCON = 00H, TR = 0 TIMER0 STOP
        MOV     TMOD,#01H     ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
        MOV     IP,#00H       ; IP = 00H
```

```
        MOV     IE,#82H         ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV     R6,#F0H
        MOV     R7,#FFH
        MOV     TL0,R6
        MOV     TH0,R7
        MOV     TCON,#10H       ; TCON = 10H, TR0 = 1, GO
        MOV     PCON,#01H       ; ENTER IDLE MODE
UPDATE_16K:
        MOV     TCON,#00H       ; TCON = 00H , TR = 0 TIM0 STOP
        MOV     IP,#00H         ; IP = 00H
        MOV     IE,#82H         ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV     TMOD,#01H       ; TMOD = 01H, MODE1
        MOV     R6,#E0H          ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 ms
                                ;DEPENDING ON USER'S SYSTEM CLOCK RATE.
        MOV     R7,#B1H
        MOV     TL0,R6
        MOV     TH0,R7
ERASE_P_4K:
        MOV     SFRCN,#22H      ; SFRCN = 22H, ERASE 16K  AP Flash EPROM
        MOV     TCON,#10H       ; TCON = 10H, TR0 = 1,GO
        MOV     PCON,#01H       ; ENTER IDLE MODE (FOR ERASE OPERATION)
;*********************************************************************
;* BLANK CHECK
;*********************************************************************
        MOV     SFRCN,#0H       ; SFRCN = 00H, READ 16KB AP Flash EPROM
        MOV     SFRAH,#0H       ; START ADDRESS = 0H
        MOV     SFRAL,#0H
        MOV     R6,#FEH         ; SET TIMER FOR READ OPERATION, ABOUT 1.5 μS.
        MOV     R7,#FFH
        MOV     TL0,R6
        MOV     TH0,R7
blank_check_loop:
        SETB    TR0                     ; enable TIMER 0
        MOV     PCON,#01H               ; enter idle mode
        MOV     A,SFRFD                 ; read one byte
        CJNE    A,#FFH,blank_check_error
        INC     SFRAL                   ; next address
        MOV     A,SFRAL
        JNZ     blank_check_loop
```

```
        INC     SFRAH
        MOV     A,SFRAH
        CJNE    A,#40H,blank_check_loop         ; end address = FFFFH
        JMP     PROGRAM_16KROM
blank_check_error:
        JMP     $
;*****************************************************************************
;* RE-PROGRAMMING 16KB AP Flash EPROM BANK
;*****************************************************************************
PROGRAM_16KROM:
        MOV     R2,#00H         ; Target low byte address
        MOV     R1,#00H         ; TARGET HIGH BYTE ADDRESS
        MOV     DPTR,#0H
        MOV     SFRAH,R1        ; SFRAH, Target  high address
        MOV     SFRCN,#21H      ; SFRCN = 21H, PROGRAM 16K AP Flash EPROM
        MOV     R6,#BDH         ; SET TIMER FOR PROGRAMMING, ABOUT 50 μS.
        MOV     R7,#FFH
        MOV     TL0,R6
        MOV     TH0,R7
PROG_D_16K:
        MOV     SFRAL,R2        ; SFRAL = LOW BYTE ADDRESS
        CALL    GET_BYTE_FROM_PC_TO_ACC  ;THIS POOGRAM IS BASED ON USER'S CIRCUIT.
        MOV     @DPTR,A         ; SAVE DATA  INTO SRAM TO VERIFY CODE.
        MOV     SFRFD,A         ; SFRFD = data IN
        MOV     TCON,#10H       ; TCON = 10H, TR0 = 1,GO
        MOV     PCON,#01H       ; ENTER IDLE MODE (PRORGAMMING)
        INC     DPTR
        INC     R2
        CJNE    R2,#04H,PROG_D_16K
        INC     R1
        MOV     SFRAH,R1
        CJNE    R1,#40H,PROG_D_16K
;*****************************************************************************
; * VERIFY 16KB AP Flash EPROM BANK
;*****************************************************************************
        MOV     R4,#03H         ; ERROR COUNTER
        MOV     R6,#FEH         ; SET TIMER FOR READ VERIFY, ABOUT 1.5 μS.
        MOV     R7,#FFH
```

```
        MOV     TL0,R6
        MOV     TH0,R7
        MOV     DPTR,#0H        ; The start address of sample code
        MOV     R2,#00H         ; Target  low byte address
        MOV     R1,#00H         ; Target  high byte address
        MOV     SFRAH,R1        ; SFRAH, Target high address
        MOV     SFRCN,#00H      ; SFRCN = 00H, Read AP Flash EPROM
READ_VERIFY_16K:
        MOV      SFRAL,R2       ; SFRAL = LOW ADDRESS
        MOV     TCON,#10H       ; TCON = 10H, TR0 = 1,GO
        MOV     PCON,#01H
        INC     R2
        MOVX     A,@DPTR
        INC     DPTR
        CJNE    A,SFRFD,ERROR_16K
        CJNE    R2,#00H,READ_VERIFY_16K
        INC     R1
        MOV     SFRAH,R1
        CJNE    R1,#40H,READ_VERIFY_16K
;*****************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*****************************************************************************
        MOV     TA,#AAH
        MOV     TA,#55H
        MOV     CHPCON,#83H             ; SOFTWARE RESET. CPU will restart from AP Flash EPROM
ERROR_16K:
        DJNZ    R4,UPDATE_16K           ; IF ERROR OCCURS, REPEAT 3 TIMES.
                                        ; IN-SYST PROGRAMMING FAIL, USER'S PROCESS TO DEAL
                                          WITH IT.
                .
                .
                .
```

24. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	November 9, 2004	-	Initial Issued
A2	December 16, 2004	58 / 60	1.To add PWM Function Description 2.To add ADC Function Description
A3	April 19, 2005	87	1. Add Important Notice
A4	June 16, 2005	3 61	Add Lead free (RoHS) part numbers Modify PWM Function block diagram
A5	September 5, 2005	- 5 53	Re-organize document Modify pin description of port 0 Modify the diagram of serial port mode 2
A6	October 3, 2005	8 9	Correct AP Flash ROM size Correct the explanation of Port 0
A7	November 16, 2005	75	Revise "Pull $\overline{EA}$ low" to "Pull $\overline{EA}$ high"
A8	March 28, 2006	16	Revise SM0 and SM1
A9	November 6, 2006		Remove block diagram
		3	Remove all Leaded package parts
		65	Revise the input current P1,P2,P3 from -50uA(Min.) to 70uA(Min.)
		65	Revise the Logic 1 to 0 Transition Current P1, P2, P3 from -500uA(Min.) to -750uA(Mmin.)
		66	Revise the Sink current P1,P3 from 10mA(Max.) to 15mA(Max.)
		66	Revise the Sink current P0,P2,ALE, $\overline{PSEN}$ from 12mA(Max.) to 15mA(Max.)

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.